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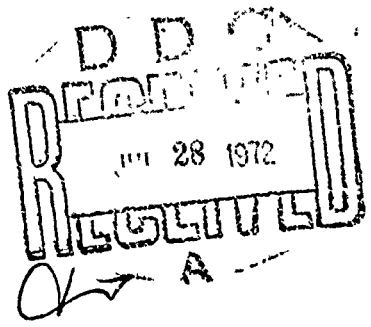
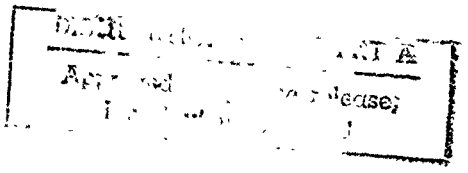


BDM FINAL REPORT VOLUME I

SEMICONDUCTOR AND NONSEMICONDUCTOR DAMAGE STUDY



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BDM FINAL REPORT VOLUME I

SEMICONDUCTOR AND NONSEMICONDUCTOR DAMAGE STUDY

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CONTENTS

SECTION 1.

DETERMINATION OF THRESHOLD FAILURE LEVELS OF SEMICONDUCTOR DIODES AND TRANSISTORS DUE TO PULSE VOLTAGES

ABSTRACT

Theoretical predictions of circuit failure in an Electromagnetic Pulse (EMP) environment require a knowledge of failure levels for each component of the circuit due to surge voltages or currents. For most circuits, the semiconductor devices are the weakest elements with respect to such failure. This section presents the results of an extensive experimental program to determine pulse power failure levels of semiconductor junctions. Approximately 110 different types of silicon diodes and transistors were studied with variations in junction areas from 10^{-4} to 10^{-1} cm^2 and with widely varying junction geometries. Power levels of up to two kilowatts, with time durations of 0.1 to 20 microseconds, were applied to semiconductor junctions in both forward and reverse polarity modes. A semi-empirical formula, based on experimental data and on a simple thermal failure model is given. From the formula one can make order-of-magnitude estimates of the failure level as a function of pulse length for many silicon diodes or transistors whose junction area is known.

Introduction

There have been extensive studies of nuclear radiation effects on electronic circuitry and systems for a variety of radiation environments. An area of increasing interest in the past few years is the effect of Electromagnetic Pulse (EMP) radiation. There are many phases in studies of EMP effects on electronic circuits. A major phase of such a study is the determination of the free-field EMP environment, and the transfer function between this environment and the system configuration under consideration. These results are used to predict the electrical signal impressed on the circuitry. Parts of these studies have been published [1]-[3] and further consideration of this phase of the overall problem is not given in this

paper. A second major phase, the subject discussed in this section, is the study of effects once the induced circuit transients are known. Using the calculated amplitude and waveshape of the induced transient as an input parameter, one can calculate the circuit behavior by use of network analysis programs designed for computer use. As a principal part of the overall prediction of EMP effects on circuitry one would like to be able to make a reasonable estimate of whether or not the circuit will properly respond once the transient conditions have passed. Such predictions require a knowledge of the levels at which the circuit components will fail due to electrical stress. In general, the semiconductor components are the most susceptible to damage by transient voltages. Good composition resistors can withstand pulse powers of better than 10,000 times their power rating for microsecond pulses. Also voltage pulses high enough to cause semiconductor damage will not damage many resistors because the current is limited to very low values by the resistance of the device.

There has been extensive work done on damage and failure mechanisms in semiconductors [4]-[9]. However, there is no general failure level information available for the extensive number of diodes and transistors used in present-day circuitry. Specifically, there is a particular lack of failure levels for microsecond and sub-microsecond pulses. Shielding circuitry in an EMP environment would become a formidable problem if the manufacturer's maximum ratings were used to establish a failure level for a device. A more logical solution is to determine the actual failure levels and shield accordingly. Also, if failure levels of components are known, then the problem of an EMP environment can be considered during circuit design and proper components chosen. The determination of failure levels is not only applicable to EMP problems but is also applicable whenever high transient voltages appear in a circuit whether the pulse origin is EMP, gamma induced, or a transient from within the system itself.

The failure level program to be described had three main objectives: (1) to determine approximate failure levels for some 110 specific semi-

conductor diodes and transistors, (2) to determine whether one could obtain a model or an empirical formulation which would enable one to calculate approximate failure levels for other devices, and (3) to calculate failure levels for the devices tested at various pulse durations for which testing was not specifically accomplished. Such empirical formulations appeared to be quite feasible based on earlier results of Davies and Gentry [10] for longer pulse durations. However, semi-empirical formulations of solutions to such a problem must be used with caution. Because of the wide variety and characteristics of semiconductor devices the analysis presented may not be valid in all cases.

Testing Philosophy

Failure levels for various pulse durations were desired for a large number of different types of devices. A large enough program to provide statistically valid data for each test was determined to be prohibitive. Therefore, the testing program was based on small samples (generally 5 to 10) of each device for each test in order to achieve a value for the general region in which threshold failure occurs. The confidence in the failure levels so obtained is greatly increased by providing a general theoretical framework in which to evaluate the experimental results. A thorough inter-comparison of the different devices is made based on their common modes of failure. Since there is an infinite number of conditions under which a transistor may be operating (i.e., different circuit connections), the transistor failure was found for each terminal pair with the third terminal open. Predominantly the emitter-base junction was tested. No steady state power or bias was applied to the transistor during tests. Failure analysis can then be correlated with circuit code predictions for the power level between each specific terminal pair.

If a device is tested in an unbiased condition, the behavior of certain microscopic processes will change. A number of junction phenomena, such as second breakdown [11]-[14], depend on the total combination of transistor

conditions. The present computer circuit code models are also not of such a nature to take into account the many complex physical phenomena occuring. Therefore, the failure level of some devices under certain operating conditions might well be significantly lower than the following analysis predicts. There has not been sufficient comparison between failure levels obtained in the manner described to those obtained in specific circuit configurations to be able to state that such analysis is always valid. However, it is not expected that the failure levels will be orders of magnitude higher because the analysis is based on the formation of microplasmas and hot spots within the junction. The presence of localized molten areas within the junction is nearly certain to cause permanent changes in the junction. Only in the cases of very small area microplasmas has full recovery been reported.

Junction Failure Modes

Because the present study involvement is concerned with high amplitude voltage pulses between two terminals of an inactive device, it is possible to examine the failure mode of a single p-n junction whether or not the actual device is a diode or a multiple junction device. However, for a more comprehensive study of possible failure modes, it is necessary to be aware of all processes that may be peculiar to the device under consideration. Such processes can depend on circuit conditions, the number and types of p-n junctions, and on general geometrical and construction details.

The failure of a solid state junction device is considered to have occurred if the parameters of any p-n junction have been seriously degraded or if the device junction has become an open or a short circuit. In a more comprehensive study one might wish to study the degree of the degradation of parameters of the device such as gain, junction capacitance, reverse saturation current, breakdown voltage levels, etc., below a certain pre-

determined level. Although the actual failure of the device is due to an opened or shorted junction, it is convenient for analysis to discuss the failure in terms of the mechanisms which eventually cause the open or short to occur. It is also convenient to divide the discussion between effects due to the application of forward or reverse voltages.

The principal breakdown mechanisms for reverse voltages on a single p-n junction are:

(1) surface breakdown around the junction, and

(2) internal breakdown through the junction within the body of the device.

The problem of surface breakdown over the junction has received considerable design consideration [10] in more recent years. With the understanding of theoretical models based on the solution of Poisson's equation with different geometrical boundary conditions, junctions have been successfully designed and built which exhibit body breakdown prior to any surface breakdown phenomenon. The problem of theoretically predicting surface breakdown is a very difficult one since it depends upon so many parameters such as geometrical design, doping levels near the surface, lattice discontinuities on the surface, and general surface conditions. The theoretical models which have been used are generally limited to the calculations of field gradients at the surface under homogeneous crystal conditions and approximate geometrical boundaries which lend themselves to theoretical calculation. Under pulse conditions, the problem is even more formidable. Davies and Gentry state, "Unfortunately the transient energy which can be dissipated during surface breakdown is both unpredictable and appreciably lower than that which can be absorbed within the body of the p-n junction device."

The actual destruct mechanism of such a surface breakdown is usually to establish a high leakage path around the junction, thus nullifying the junction action. The actual internal junction itself is not necessarily destroyed as has been shown since re-etching the surface can return the diode to normal

action. In internal body breakdown the destruct mechanism apparently results from changes in the junction parameters due to the high temperatures locally within the junction area. These temperatures can be of such magnitude that alloying, or diffusion of the impurity atoms, occurs to such an extent that the junction is either totally destroyed or its properties drastically changed. Figure 1.1 shows four mechanisms for the movement of impurity atoms through a lattice.

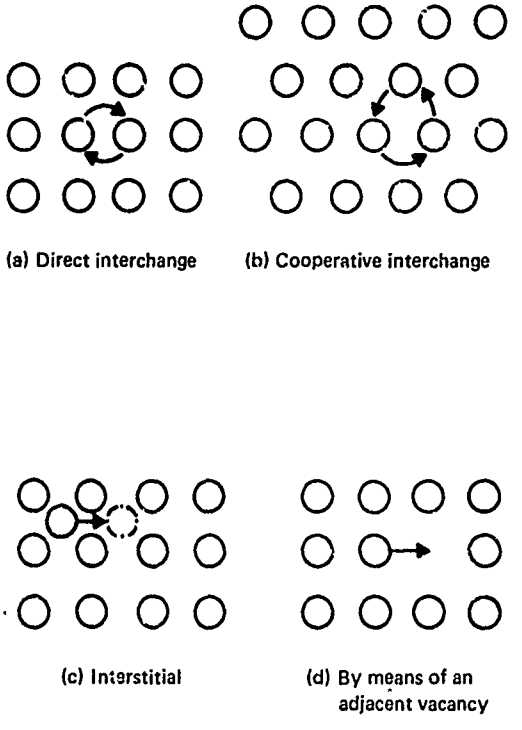

Figure 1.1 Mechanisms of Movement of Impurity Atoms through a Lattice.

Of the four mechanisms depicted, (a) direct interchange, (b) cooperative interchange, (c) interstitial, and (d) adjacent vacancy, the last two are predominant in silicon.

High temperatures and strong applied fields as well as the density gradient aid the movement through the lattices.

In many cases both for forward and reverse voltages the current is sufficiently high and localized to cause melting at hot spots [4]-[9] within the junction. Such action can result in a resistive path across the junction which masks any other junction action.

For long term heating at temperatures well below the melting level impurity diffusion can be an important mechanism contributing to device degradation. For very short pulses hot spot formation is more likely the predominant cause of failure.

Junction failure can also occur due to dielectric breakdown. The large avalanche current can form a path for an arc discharge to occur. This can result in a puncture through the junction with an actual pin hole being formed. Usually a junction short results. This effect will be described as a puncture rather than "punch-through" reserving the latter term for a depletion width phenomena occurring in multiple junction devices.

For forward voltages surface breakdown is not expected to be a problem. The field gradients on the surface across the junction are normally quite small since the junction is in a highly conducting state.

The failure of the junction for forward voltages is then expected to be primarily due to the temperature rise due to the high currents passed during the pulse. The destruct mechanism being mainly the change in junction parameters due to the high temperatures as discussed for reverse voltages.

To illustrate a condition in which the operating conditions are important, the breakdown mechanism occurring in transistors called punch-through will briefly be discussed. If the base region is of higher resistivity than the collector region, the depletion region of the collector-base junction extends mainly into the base region. As the collector voltage is increased, the depletion region extends further and further into the base region. If the base region is very thin, then the collector voltage may be high enough to cause the depletion region to extend entirely through the base and make contact with the emitter-base depletion region thus effectively causing a short across the base region. This will occur if the collector voltage necessary to extend the depletion region through the base is smaller than the voltage required to

initiate avalanche breakdown. Again, if the current is limited there is no permanent damage done to the transistor due to the punch-through. When the collector voltage is decreased the transistor will return to normal action.

The pulse rise time also may affect the breakdown characteristics of a junction. Experiments by Agatsuma, Kohisa, and Sugiyama [15] on the collector to emitter breakdown with the base open showed that the energy required to initiate second breakdown was much less with fast rising pulses. One theory is that if the voltage rise is slow, the breakdown occurs over the whole junction area. If the voltage rise is very fast, it appears that very localized breakdowns occur within the junction which then carry very large currents. Ioffe and Regel [16] give the conductivity of molten silicon as about 10^4 $ohm^{-1} - cm^{-1}$ which is about 30 times greater than the solid at the melting point. Thus, appreciable currents can be conducted by small areas of the junction. Localized hot spots occur and the temperature rise can be great enough to cause permanent damage. This can occur at pulse energy levels much below the energy levels required to cause damage with slow rising pulses.

Considering nanosecond rise-time pulses, it could be expected that the reverse voltage breakdown level would become appreciably higher since the rate of rise could be appreciably faster than the time required to initiate breakdown. Experimental results published by Portnoy and Gamble [17] for collector-emitter breakdown with the base open show that voltages above breakdown can be applied for fairly long times (tens of microseconds) without breakdown. If the pulse continues for longer times, the junction breaks down and the voltage drops to the calculated breakdown voltage.

Also, depending on the pulse rise time and width, other parameters such as the skin effect, non-homogenous local fields, emitter crowding and ion migration may affect the failure levels.

Modeling for Junction Failures

Although many different microscopic mechanisms occur, it has been found that most of these failure mechanisms are linked primarily to the

junction temperature. Therefore, the theoretical treatment of the problem can be reduced to a thermal analysis. The pulse times considered in this study are 0.1 to 20 microseconds. For these short times, the boundaries of the bulk material and the thermal heat sinks do not have the effect they would at longer times. The junction temperature can be adequately approximated from simple linear heat flow theory. Although more exact thermal models have been devised [10], [18]-[20] to account for specialized boundary conditions, the attempt here is to use an intermediate model that is reasonable for a wide variety of devices. In this manner the experimental results for different devices and pulse duration can be readily compared. There is no doubt that a better model could be made for any one specific device if sufficient information on the junction parameters such as geometry, thickness, doping, resistivity, and the geometry of the device as a whole were available. Investigations were not made during this study to attempt to relate failure to any of these other parameters.

Microplasmas and hotspot information are presently being investigated and results reported by many authors. As better three-dimensional models of hotspot formation are made, better estimates of junction burnout as a function of pulse width may be made. One of the principal problems of three dimensional solutions is the need for more exact information about the geometry of the devices. Generally such information is not readily available. Other models of the temperature rise of hotspots may give a slightly different time dependance. It is felt that the time dependance of $t^{-1/2}$ derived here is appropriate and sufficiently accurate for the pulse times considered. The two dimensional model derived by Takagi and Mano [20] gives a maximum current time dependance of $t^{-1/4}$ and hence a power dependance of $t^{-1/2}$. The worst case as far as achieving high temperatures in the junction is when one considers that all of the power dissipated in the device occurs in the junction. This corresponds physically to the situation where a high-voltage pulse of reverse polarity is applied to a junction with a high reverse voltage breakdown. When the avalanche breakdown occurs, almost all of the applied voltage

is dropped across the junction, and only a small percentage is dropped across the bulk material. For such a thermal model, the junction failure conditions (derived in Appendix A) are

$$P/A = \sqrt{\pi \kappa \rho C_p}\,[T_m - T_i]\, t^{-1/2}, \tag{1}$$

where P is the power; A, the junction area; κ, the thermal conductivity; ρ, the density; C_p, the specific heat; T_m, the failure temperature, T_i, the initial temperature; and t, the time. This equation is of similar form to that suggested by Davies and Gentry [10]; its simple form leads to many distinct advantages in general use. Equation (1) is plotted for three specific cases in Fig. 1.2:

Case I - Heating from approximately room temperature of 25°C to 675°C which is the model failure temperature suggested by Davies and Gentry and is also within the temperature range discussed by other authors [4], [9].

Case II - Heating from 25°C to the approximate melting temperature of silicon of 1415°C.

Case III - Identical to Case II except that the currents are assumed to pass through localized hot spots which account for one-tenth the total junction area. This choice provides a convenient reference when intercomparing data since the curves for Case II and III are exactly separated by one order of magnitude.

The form of the solution has many advantages such as: (1) It is a straight line on log-log plots and hence allows a quick estimate of failure levels by plotting the power versus pulse time duration for a known junction area. This is in contrast to more exacting models whose solution is usually of the form of an infinite series and require more exacting information about the specific geometry of the device. (2) The only physical parameter needed for a specific device is the junction area. (3) It is simple to use as a semi-empirical

equation to match specific experimental data by keeping the appropriate slope of -1/2 and adjusting the constant to best fit the data. It is possible to determine the constant from the curves shown by merely reading off the value of the power per unit area at the one microsecond pulse duration provided the curves are plotted in units of kilowatts/sq.cm. and microseconds. (4) It allows an intercomparison of devices of different junction areas and various junction geometries by plotting the power per unit area for failure for the different devices all on a single plot.

In order to utilize these advantages, the solution was also used to compare data in those cases for which it was not used as an appropriate model. Two examples of this are (1) devices where the reverse breakdown voltage is small and (2) when the greater percentage of the applied forward voltage is dropped across the bulk material rather than the junction. In such cases the actual temperature of the junction is lower than the model implies. However, for the pulse durations under consideration, the calculated slope is still approximately valid and when comparison is made between the theoretical curves and the experimental data, the experimental curves will prove to be higher. If the reverse failure levels are used for all cases it merely gives a slightly conservative estimate for the forward voltage mode. At very short pulse durations (sub-microsecond) extremely large powers are required to obtain failure. Hence in many cases large currents are required with the result that significant amounts of power are dissipated throughout the bulk semiconductor. In such short times the heat transfer to the junction from points away from the junction is very small. For such cases the temperature of the junction approaches a dependenc. more like $1/t$ rather than $1/\sqrt{t}$. However, within the time scales studied the deviation was not sufficient to justify a separate model. Again, . the failure levels presented are on the conservative side for very short times.

An inherent limitation of the power failure model is the fact that actual failure modes are not one dimensional heat flow processes, and the simple theory cannot be expected to give exacting answers. However, certain of the

assumptions tend to have a cancelling effect. For example, phase change energy considerations and bulk heating (for devices where the reverse breakdown voltage is small or in the case of forward applied voltages) would raise the power curve of Fig. 1.2, while hot spot formation over less than one-tenth the total junction area would lower it. The experimental data supports the use of the theoretical estimates even with such a wide range of junction geometries and areas, failure mechanisms, and thermal boundary conditions.

To perform a complete theoretical failure analysis it is required to know the power being delivered to the semiconductor junction. This involves calculating the voltage and current levels for the junction. For this program, the power levels for failure were determined experimentally. Therefore, a thorough discussion of models for junction voltage and current levels will not be made. A very brief discussion of some of the basic approaches to voltage and current calculations is given in Appendix A.

Experimental Conditions and Results

All of the devices were tested to determine the threshold failure level of semiconductor junctions due to a high electrical stress. The general procedure consisted of step voltage pulsing the junction until failure or degradation of the device occurred. In the majority of the failures, a single pulse reduced the DC Beta and the zener voltage to zero with the device assuming a resistor characteristic. Pulse power levels of up to 2 kilowatts (a few peaks to 8 kilowatts) were applied with pulse times of 100 nanoseconds to 20 microseconds. The risetime of the applied pulse was approximately 20 nanoseconds. For each pulse, the waveform of the current through and the voltage across the device were recorded photographically. The photographic data was reduced to show the power level and the pulse duration applied to the terminals of the device. Figures 1.3 and 1.4 show typical photographs for a reverse polarity pulse applied to a junction. The pulse in Fig. 1.3 caused no damage. The pulse in Fig. 1.4 caused the junction to fail during the time that the pulse was applied. The applied

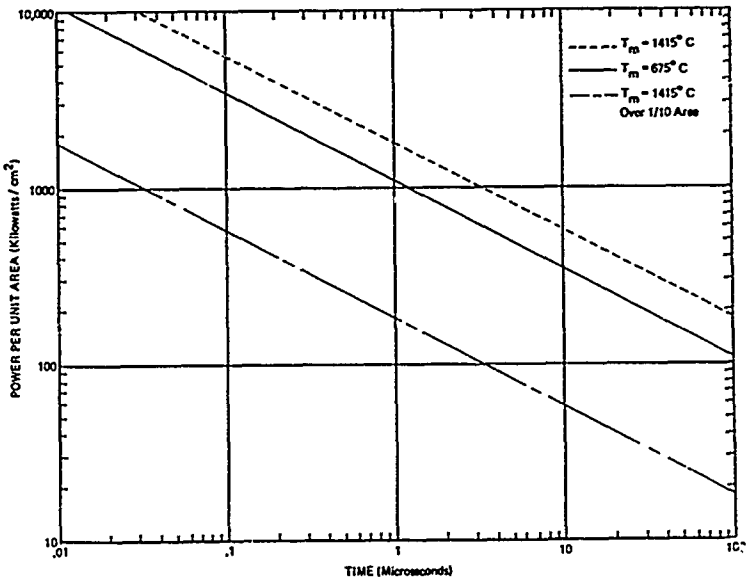

Fig. 1.2. Theoretical failure curves for silicon junctions for reverse polarity voltage.

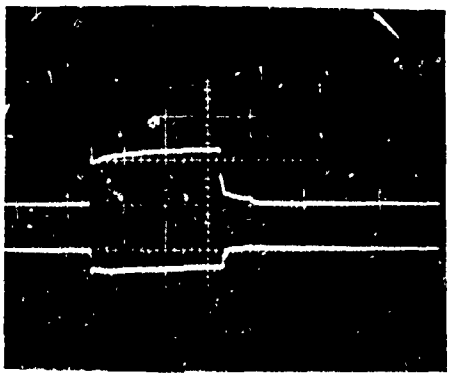

Fig. 1.3. Voltage - Current traces for a semiconductor junction under an applied reverse voltage pulse. (a) Voltage - 100 v/cm, (b) Current - 5 a/cm, sweep speed - 2 μ sec/cm.

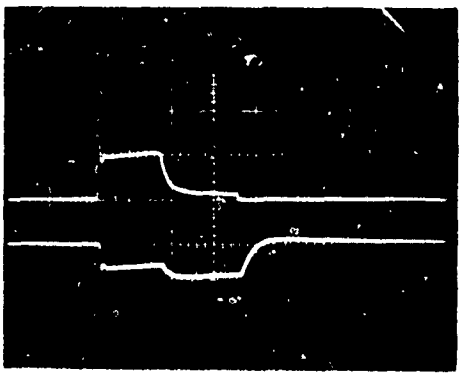

Fig 1.4. Voltage - Current traces for a semiconductor junction under an applied reverse voltage pulse. (a) Voltage - 100 v/cm, (b) Current - 5 a/cm, sweep speed - 2 μ sec/cm.

pulse time was approximately the same in both figures. Figure 1.4 shows that when the junction failed the voltage across the terminals dropped by approximately the value of the reverse breakdown voltage of the junction.

An attempt to determine the mode of failure on each device was not made. However, a number of devices were examined after failure. In each case where the damage was evident, it appeared that localized melting had occurred. In some devices sufficient melting had taken place that a flow of melted silicon could be observed. From these results and the information of other investigators [4]-[9], it is believed that the predominant failure mode, for these microsecond and sub-microsecond pulses, is localized melting across the junction. The melted regions form resistive paths across the junction which shorts out or masks any other junction action.

Since most devices tested required greater power for failure in the forward voltage mode, the experimental measurements were concentrated primarily on the reverse voltage mode.

Figures 1.5 and 1.6 are power versus pulse duration plots for two specific diodes. The line on each plot is a line with a slope of -1/2, which best fits the data taking into account both failure and no failure points and uncertainty in the data for each point. The purpose of the figures is to give an indication of the actual power levels and the spread of points which caused failure. The plots illustrate that the time dependance is based on the total semi-empirical analysis rather than from the few data points obtained for each device.

It was impossible to achieve a variation in burn-out time for several diodes tested for the reverse polarity voltage case. Normally a variation in burn-out time was achieved by reducing the amplitude of the applied voltage pulse. Also, when many of these diodes failed, the power level was below that previously dissipated without damage. A possible explanation for these results is as follows: Because of the geometrical uniformity of the diode, normally a large area of the junction is conducting and carrying the reverse current. Therefore, larger powers can be dissipated without failure

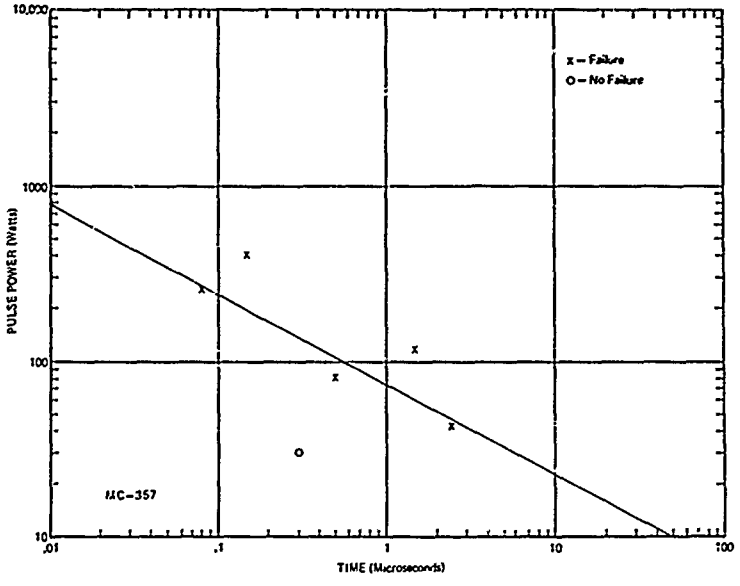

Fig. 1.5. Experimental data points for failure of the anode-cathode junction of a MC-357 diode for reverse polarity voltage pulses.

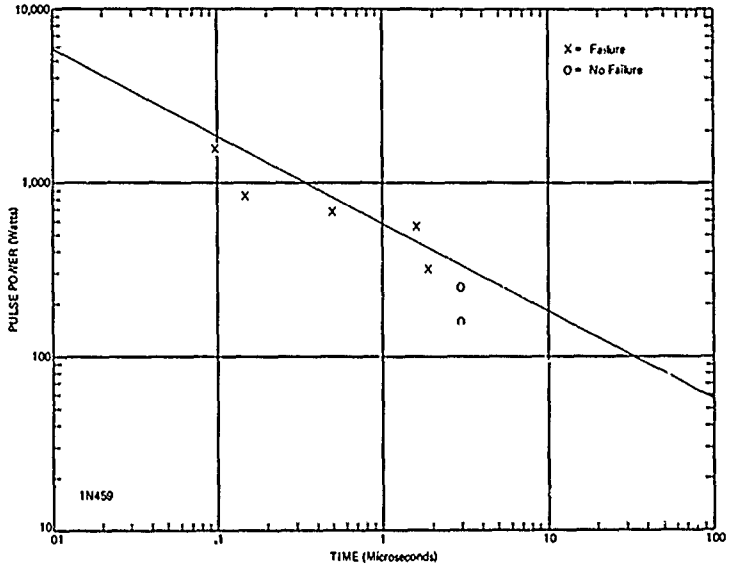

Fig. 1.6. Experimental data points for failure of the anode-cathode junction of 1N459 diode for reverse polarity voltage pulses.

as local hot spots are not as likely to form. However, as the temperature of the junction increases and a certain voltage level is reached, small differences in the junction cause sufficiently high local field gradients that a dielectric breakdown occurs or the current is channeled into localized areas. When this happens, a local hot spot quickly develops and the device burns out. If this type of mechanism is occurring, longer burn-out times at smaller power levels could be achieved by using a pulser which contained current limiting circuitry. In a few of these devices the oscilloscope photographs would indicate that junction failure had occurred; however, when tested, junction action would still be present although the device would be very leaky. Possibly very microscopic breakdowns form a high resistance (low compared to the normal reverse resistance) path instead of a complete short across the junction.

Figures 1.7 to 1.10 are power versus pulse duration plots for four transistors. Figures 1.7 and 1.8 show both forward and reverse voltage failure points for the base-emitter junction. Figure 1.8 also includes damage levels for the collector-emitter terminals. It should be noted that while the collector-emitter terminals involve two junctions, the failure level lies within the general failure region for a single junction. For the collector-emitter case it was found that either one or both junctions failed.

Figure 1.11 shows a composite of the failure points for six types of semiconductor diodes inter-compared by plotting the power per unit area for failure versus pulse duration. Figure 1.12 shows a composite of base-emitter junction failure points for eight types of transistors inter-compared on a power per unit area basis. Figure 1.13 shows a composite of ten large area diodes for which failure points were not achieved. It was impossible to cause failure in some of the large area diodes because of the current limitation of the pulser. Because of the small reverse voltage breakdown for many of these diodes, large currents of the order of 30 to 40 amps can be carried without damage. Several other diodes could not be damaged because of the voltage limitations of the pulser (1KV maximum) and the high peak inverse voltages of the devices. The reverse voltage breakdown levels of these diodes were either not reached or were only slightly exceeded with the microsecond

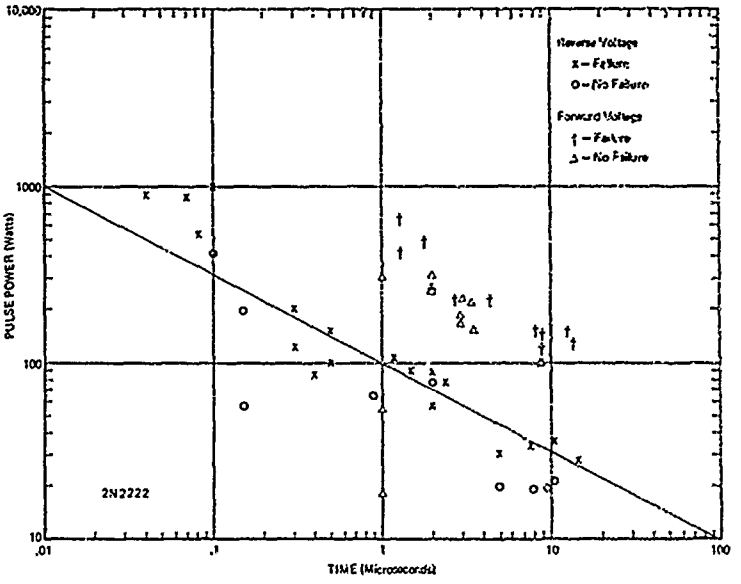

Fig. 1.7. Experimental data points for failure of the base-omitter junction of a 2N2222 transistor for forward and reverse polarity voltage pulses.

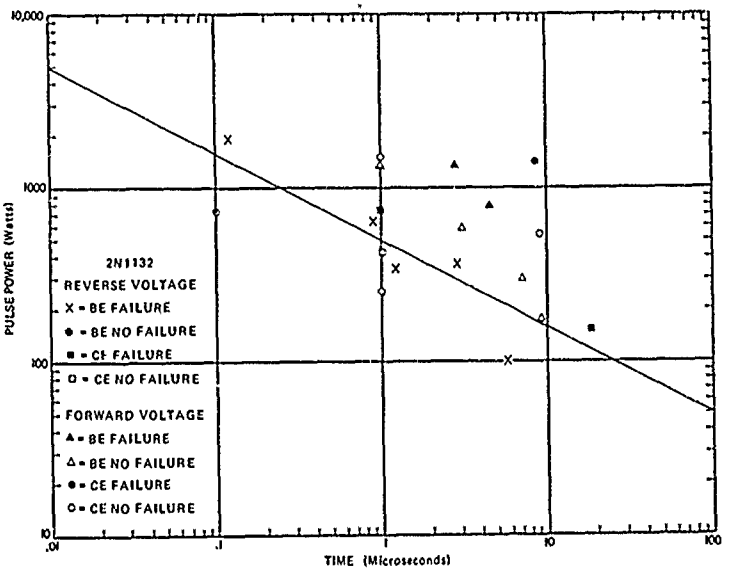

Fig. 1.8. Experimental data points for failure of the base-emitter and collector-emitter junctions of a 2N1132 transistor for forward and reverse polarity voltage pulses.

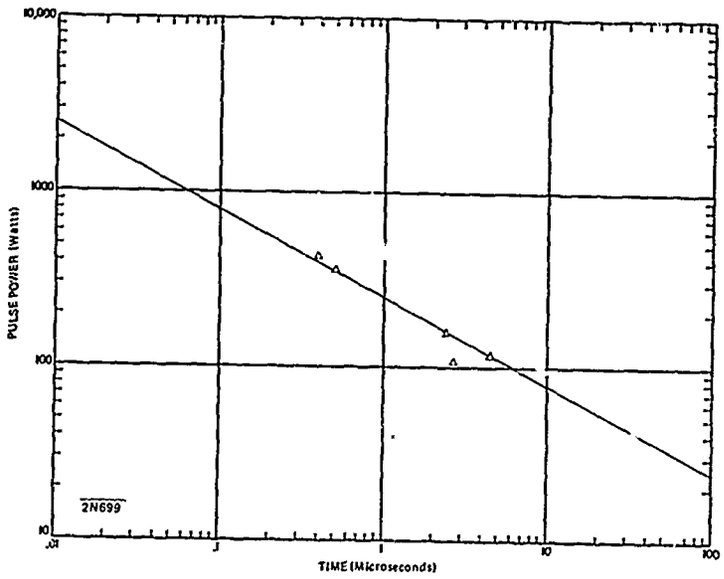

Fig. 1.9. Experimental data points for failure of the base-emitter junction of a 2N699 transistor for reverse polarity voltage pulses.

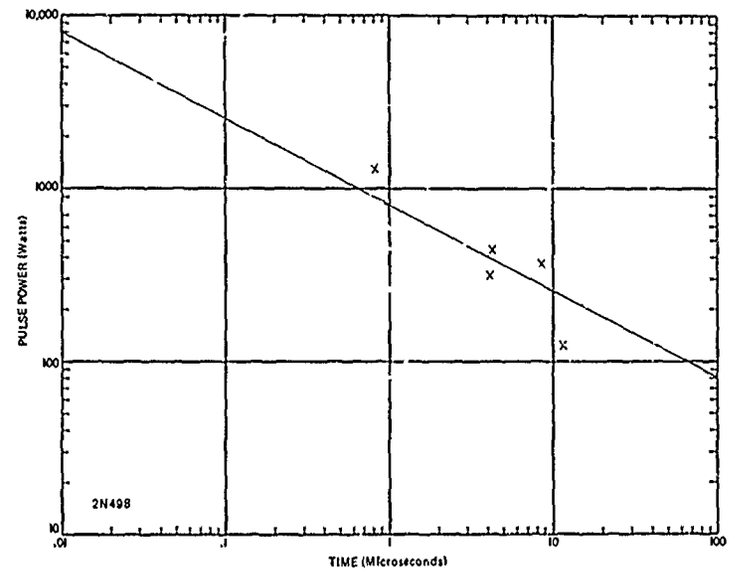

Fig. 1.10. Experimental data points for failure of the base-emitter junction of a 2N498 transistor for reverse polarity voltage pulses.

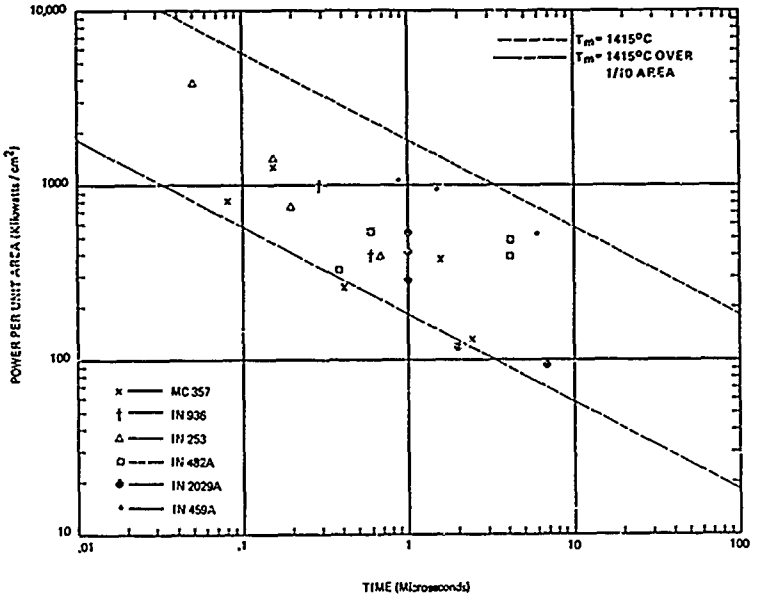

Fig. 1.11. A composite of experimental data points for the failure of the anode-cathode junction for six diodes. Inter-comparison is made by plotting power per unit area versus pulse duration. Also shown are the theoretical failure curves.

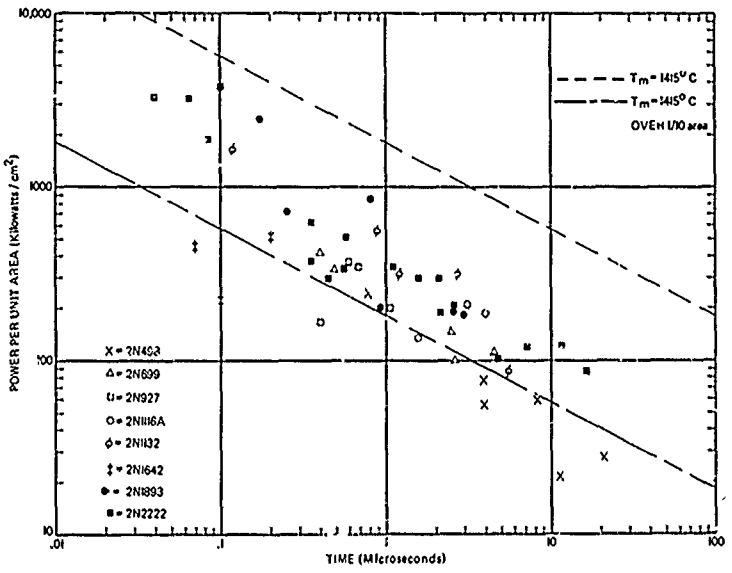

Fig. 1.12. A composite of experimental data points for the failure of the base-emitter junction for eight transistors. Intercomparison is made by plotting power per unit area versus pulse duration. Also shown are the theoretical failure curves.

pulses. Therefore, no damage to the diodes was possible with the low currents that resulted. In Fig. 1.13, the power per unit area levels shown are generally all below the power per unit area levels for which failure was observed in other similar devices. There is no certainty that these devices would not be damaged if these higher power levels had been reached.

Some of the plots of power per unit area versus pulse duration may be somewhat in error because of the uncertainty in determining the junction area. Approximately one-third of the area values for the tested devices were obtained from the manufacturer; the remaining were calculated from physical measurements of the devices. It is felt that no serious misinterpretation could result in an errant junction area calculation since a departure from an actual area value by a factor of two would not result in a change any greater than the spread of points already existing.

Figure 1.14 shows a composite of the failure points for a 2N2222 transistor tested under this program and data from a paper by Davies and Gentry [10] who gave failure points for some longer duration pulse lengths. The data is in general agreement for nearly six orders of magnitude in pulse duration.

Each of the damage lines similar to those shown in Figs. 1.5 to 1.10 were converted to a power per unit area basis. The constant for these lines was then averaged to find the best fit for all of the devices tested. The resulting equation is

$$P/A = 510t^{-1/2} \qquad (2)$$

where, for the time given in microseconds, P/A is in units of kilowatts/cm^2. Shown in Figure 1.15 are lines obtained by averaging the diode and transistor results separately. The equations for these lines are:

$$P/A = 554t^{-1/2} \qquad (3)$$

and

$$P/A = 470t^{-1/2} \qquad (4)$$

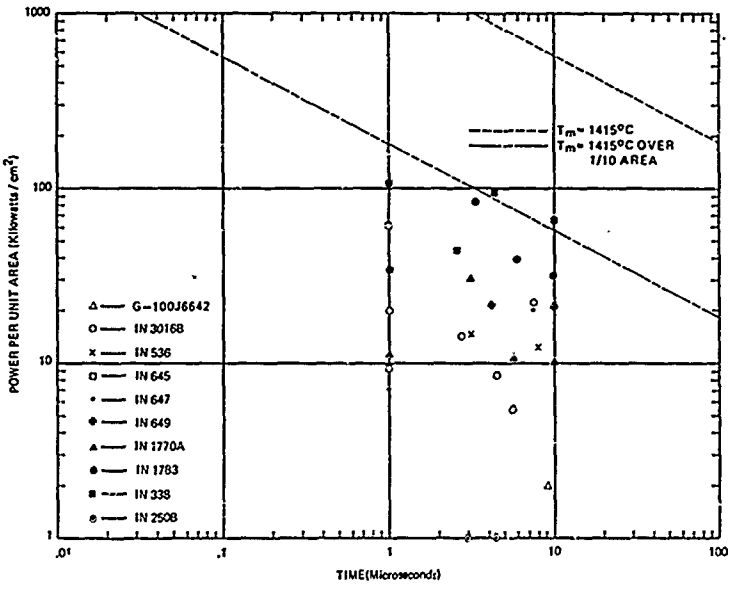

Fig. 1.13. A composite of experimental data points for which no failure was achieved for the anode-cathode junction for ten large area diodes. Inter-comparison is made by plotting power per unit area versus pulse duration. Also shown are the theoretical failure curves.

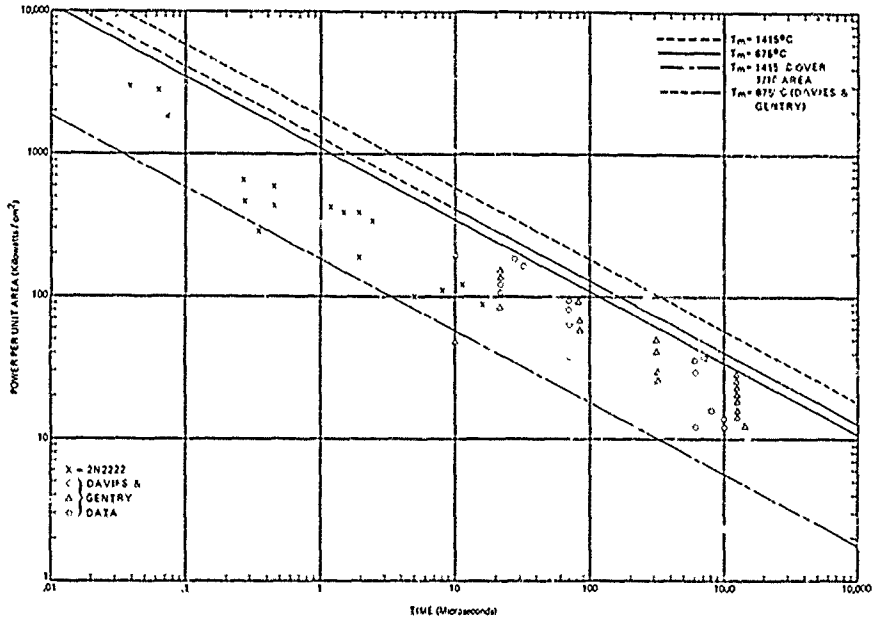

Fig. 1.14. A comparison of experimental data points for a 2N2222 transistor and points from a paper by Davies and Gentry [10]. Also shown are the theoretical failure curves from this paper and the curve by Davies and Gentry.

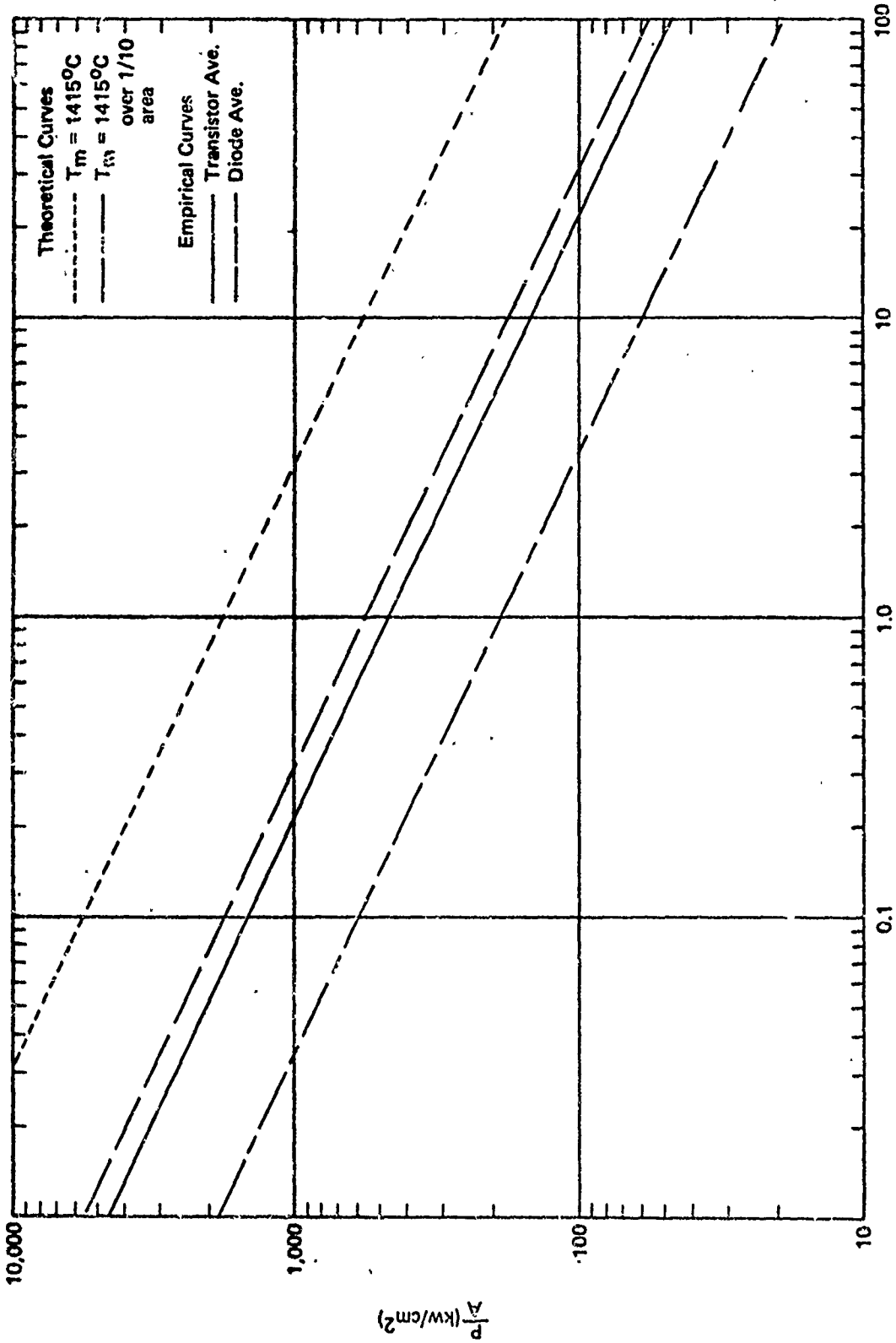

FIGURE 1.15. Standard $\frac{P}{A}$ vs Time Curves

respectively. By using the above equations and the approximate junction area, a very good order of magnitude estimate of the failure level for most silicon diodes and transistors can be calculated.

Table 1.1 gives values, for nineteen specific diodes, of the pulse power for a one microsecond pulse required to cause junction failure. The values range from 73 watts for a 1N2929A, a small silicon tunnel diode, up to 2.1 kilowatts for the 1N711A, a 7 volt zener diode.

Table 1.2 gives similar values for eighteen specific transistors. The values range from 45 watts for a 2N930, a small planar NPN transistor, up to 2.3 kilowatts for an R22705638, a large area NPN transistor.

Table 1.3 gives some typical experimental values of terminal voltage and current that caused failure for several diodes. The values range from high voltages of 1000 volts and small currents of 1 amp for high reverse breakdown diodes to low voltages of 22 volts and high currents of 36 amps for a low voltage (6.2 volts) zener such as the 1N753A. Also shown are some typical voltage and current values for forward polarity tests. For most of the forward tests high currents of up to 40 amps could be drawn without failure for large area diodes.

Table 1.4 shows similar values of voltages and currents for several transistors.

Application of Results

Computer circuit analysis codes such as CIRCUS, SCEPTER, NET-I, etc. [18], are used to correlate the experimental failure analyses with specific circuit conditions. The elements of the circuit or system are arranged in nodal fashion to reproduce the circuit in the computer program. In the operation of these codes, equivalent circuit models for the semiconductor devices are available from internal programming or as external inputs. The experimental equivalent circuit parameters for the specific semiconductor devices and the calculated amplitude and waveshape of the transient signal at some node in the circuit complete the input information necessary for the

DIODE TYPE	NOMINAL FAILURE POWER (WATTS) ~ 1 μ SEC. PULSE
W6807WS	2200
W6807ZV	2200
1N711A	2100
1N823	1800
G129	1700
1N816	1500
1N981B	1400
1N753A	1200
1N702A	1000
1N459A	960
1N482A	960
1N540	930
1N1095	880
1N253	860
1N967B	730
1N537	510
DHD936	140
MC357	74
1N2929A	73

TABLE 1.1 Pulse Power for one Microsecond Pulse required for Reverse Polarity Junction Failure.

TRANSISTOR TYPE	NOMINAL FAILURE POWER (WATTS) ~ 1 μ SEC. PULSE
R22705638	2300
R22707547	1900
MIS 17181/1-1	1500
2N657A	1070
2N1116A	980
2N498	800
2N657	620
2N335	550
2N336	550
2N1132	500
2N1893	400
2N336A	340
2N699	250
2N1642	130
2N2222	110
2N736	100
2N927	96
2N930	46

TABLE 1.2 Pulse Power for one Microsecond Pulse Required for Reverse Polarity Base-emitter Junction Failure.

DIODE TYPE	TYPICAL REVERSE FAILURE LEVELS (~0.5 - 2μ SEC. PULSE)		TYPICAL FORWARD LEVELS (~0.5 - 2μ SEC. PULSE) (No Failure Unless Noted)	
	Terminal Voltage (Volts)	Current (Amps)	Terminal Voltage (Volts)	Current (Amps)
W6807WS	1000	2	5	39
1N711A	72	28	15	36
1N823	29	36	25	34
G129	40	28	4	10
1N816	710	2	19	39
1N981B	175	8	29	30
1N753A	22	36	11	38
1N702A	20	30	14	33
1N459A	1000	0.9	15	36
1N482A	800	1	16	36
1N1095	800	1.6	9	35
1N967B	50	14	12	31 Failed
1N537	1000	1	32	40
DHD936	120	1.5	10	16 Failed
MC357	160	0.5	15	6 Failed
1N2929A	10	8.5	7	8 Failed

TABLE 1.3 Values of Terminal Reverse Voltage and Current That Caused Junction Failure.

TRANSISTOR TYPE	TYPICAL REVERSE FAILURE LEVELS (~0.5 - 2μSEC. PULSE)		TYPICAL FORWARD LEVELS (~0.5 - 2μSEC. PULSE) (No Failure Unless Noted)	
	Terminal Voltage (Volts)	Current (Amps)	Terminal Voltage (Volts)	Current (Amps)
R22705638	55	35	12	36
2N1116A	70	14	28	30
2N498	55	24	20	32
2N657	62	14	22	39
2N335	70	6	50	15
2N1132	80	8	16	16 Failed
2N1893	24	14	15	14
2N699	68	1.6	--	--
2N1642	130	1	--	--
2N2222	38	3	10	14 Failed
2N736	10	6	--	--
2N927	320	0.25	--	--
2N930	30	1.5	20	19 Failed

TABLE 1.4 Values of Terminal Reverse Voltage and Current That Caused Base-Emitter Junction Failure.

computer program to analyze the response of the circuit. The computer calculates the time history of current through and voltage across any two terminals of semiconductor devices and then plots a time history of the power dissipated. The calculated pulse length and power information form the circuit code is correlated with experimental semiconductor failure curves to estimate failure of the semiconductor device due to the specific transient being studied.

The circuit codes and failure levels are also useful in circuit design. Specific environments can be considered during the design phase and proper components chosen. Additionally, circuit reliability can be increased by incorporating protective circuitry where weak components exist.

Conclusions

It is acknowledged that while the approximate theories presented in this discussion are able to correlate a large body of experimental data, the phenomena involved are of such a complex nature that it cannot be presupposed that such a theory is applicable in all cases. To be useful, order of magnitude estimates must be used judiciously within the framework for which they were obtained. The mechanisms involved in microplasma and hot spot formation can be significantly affected by steady state operating conditions, structural geometry and to some extent by transient pulse waveshape. At longer and shorter pulse lengths the model described is not as appropriate. Even in the sub-microsecond times presented here there is evidence that the curves are not holding to a strict $t^{-1/2}$ dependence. This is partially due to the basic one-dimensional model and partially due to the large amounts of power being dissipated in the bulk material rather than at the junction. Direct surface effects and breakdown are also not covered in this analysis. Surface effects do not necessarily require high junction temperatures to cause gain degradation [22]. Veloric and Prince [23] state: "Experiments show that devices which show surface breakdown will collapse

at power levels which are orders of magnitude below that observed for devices in which body breakdown is observed."

Application of the analysis presented can produce satisfactory results providing the exceptional cases are recognized.

Summary

A simple thermal model was used to obtain estimates of semiconductor junction failure and provides the time dependence for a semi-empirical equation. This equation represents a best fit to experimental results from over 1000 devices of approximately 110 different types. The semi-empirical relation is $P/A = 510t^{-1/2}$, where, for the time given in microseconds, P/A is in kilowatts/cm^2. Actual failures on all types of devices tested were within better than one order of magnitude to the curves predicted by the thermal model and even closer to the semi-empirical equation. The semi-empirical failure equation is useful in that it allows for quick estimates of junction failure both for circuit design and for studies of electrical transients on existing circuitry. The equation can be used on most all types of silicon diodes and transistors whose junction area is known.

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SECTION 2

ESTIMATES OF SEMICONDUCTOR FAILURE DUE TO MULTIPLE VOLTAGE PULSES

Previously, we have made estimates of semiconductor failure for a single applied voltage pulse. These estimates were based on thermal failure using a simple model to determine the temperature of the semiconductor junction as a function of the pulse power and duration. Semiconductor devices were also tested for failure in the laboratory using a single voltage pulse. However, under certain conditions, one is interested in the failure level from a voltage wave which contains multiple pulses. This can arise directly from the induced EMP wave which may have a waveform as shown in Fig. 2.1 or it may arise from the circuit

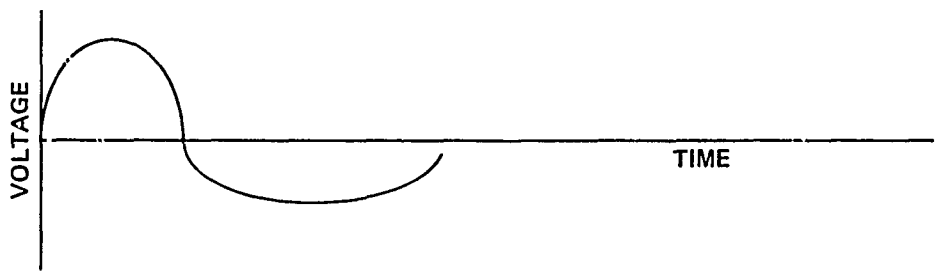

Figure 2.1

response due to a step input. Such a circuit response may be of the form shown in Fig. 2.2.

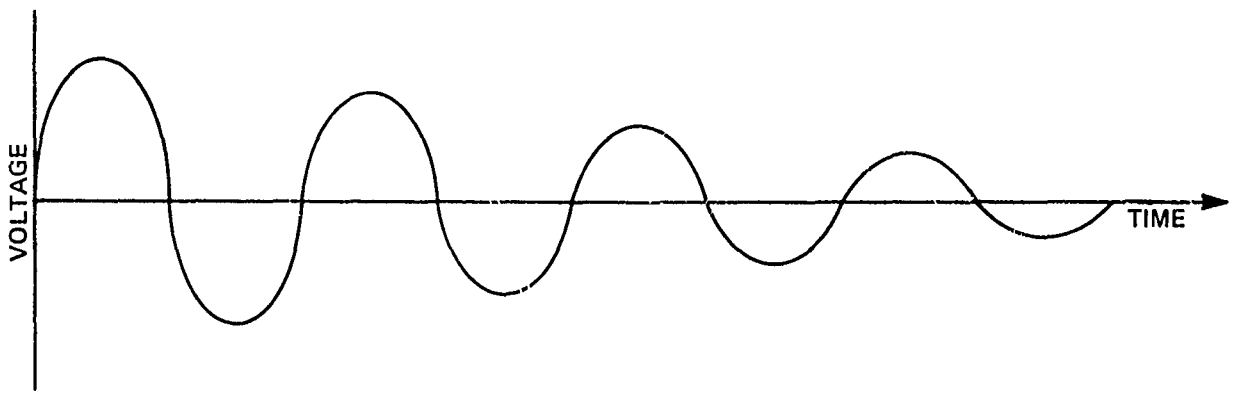

Figure 2.2

Our problem, then, is to estimate how such waveforms change the failure levels previously predicted for a single pulse. First, we will discuss some failure estimates based on our original failure model. Secondly, we will discuss some of the failure mechanisms which may be occurring and how these might cause the actual failure level for multiple pulses to differ from the predicted levels.

Since semiconductor devices are not bilateral devices, we need to consider several possible cases separately as representative of what the operating conditions might be.

Operating modes:

1. Diode with high reverse voltage breakdown--First pulse in forward direction--very small reverse conduction.
2. Diode with high reverse voltage breakdown--First pulse in reverse direction--very small reverse conduction.
3. Diode with low reverse voltage breakdown or Base-Emitter junction of transistor--First pulse in forward direction--appreciable reverse conduction.
4. Diode with low reverse voltage breakdown or Base-Emitter junction of transistor--First pulse in reverse direction--appreciable reverse conduction.

Our thermal model is bilateral since it is based on the power dissipated in the junction; therefore, we need to know the power dissipated in the junction for a given applied voltage waveform. Figure 2.3 shows the general waveforms one could expect for the four cases given above.

For cases 1 and 2, there is a very small amount of power dissipated during the time the device is under a reverse voltage pulse. For cases 3 and 4, current is flowing all the time since we have assumed that the reverse breakdown voltage is small compared to the applied voltage. For most cases, more power is dissipated directly at the junction when the device is conducting in the reverse direction. This occurs because of the much larger voltage drop across the junction in the reverse direction.

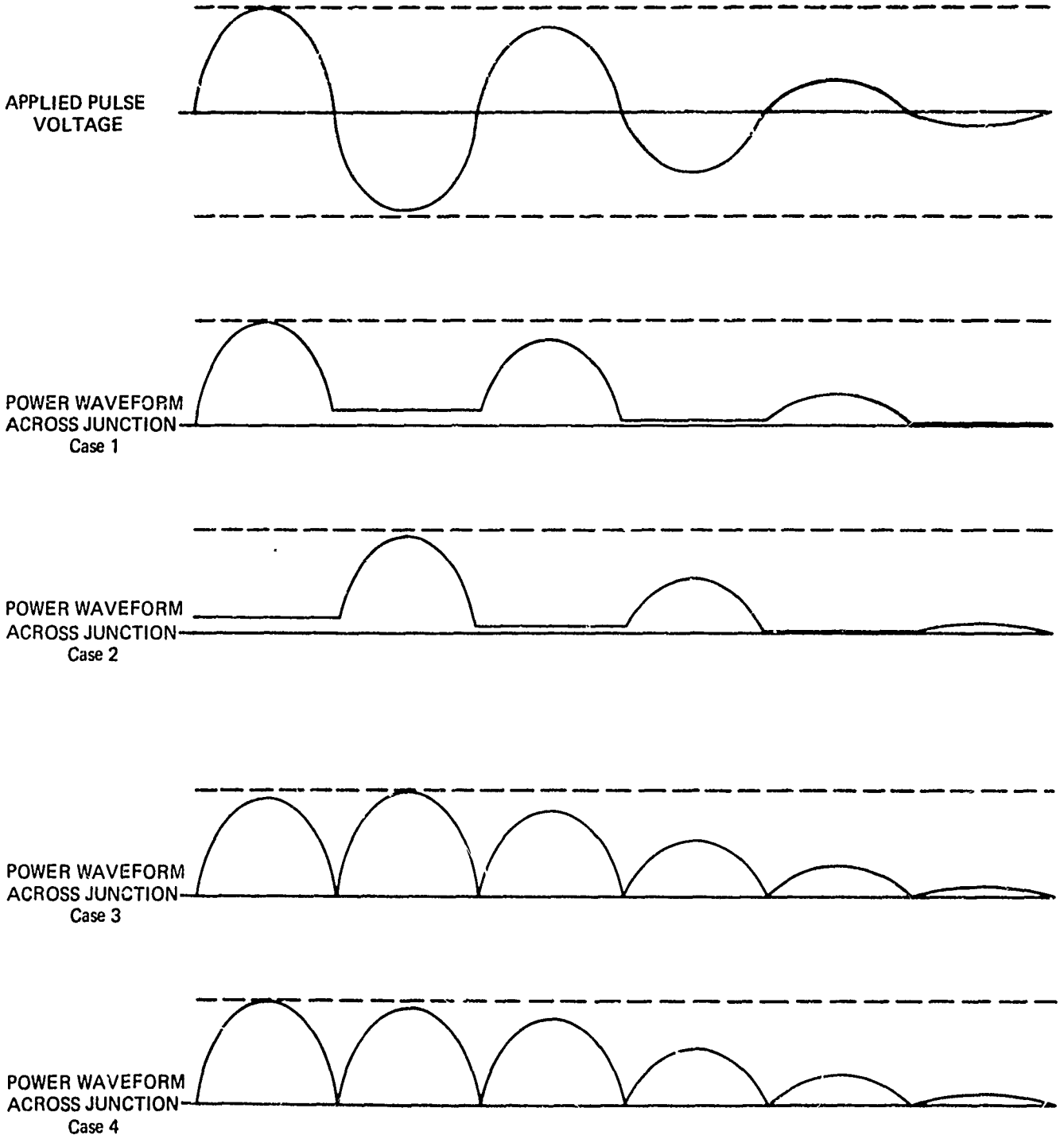
APPLIED PULSE VOLTAGE
POWER WAVEFORM ACROSS JUNCTION Case 1
POWER WAVEFORM ACROSS JUNCTION Case 2
POWER WAVEFORM ACROSS JUNCTION Case 3
POWER WAVEFORM ACROSS JUNCTION Case 4

Figure 2.3

To simulate the above power waveforms in our theoretical model, we will calculate failure for the following types of cases as shown in Fig. 2.4.

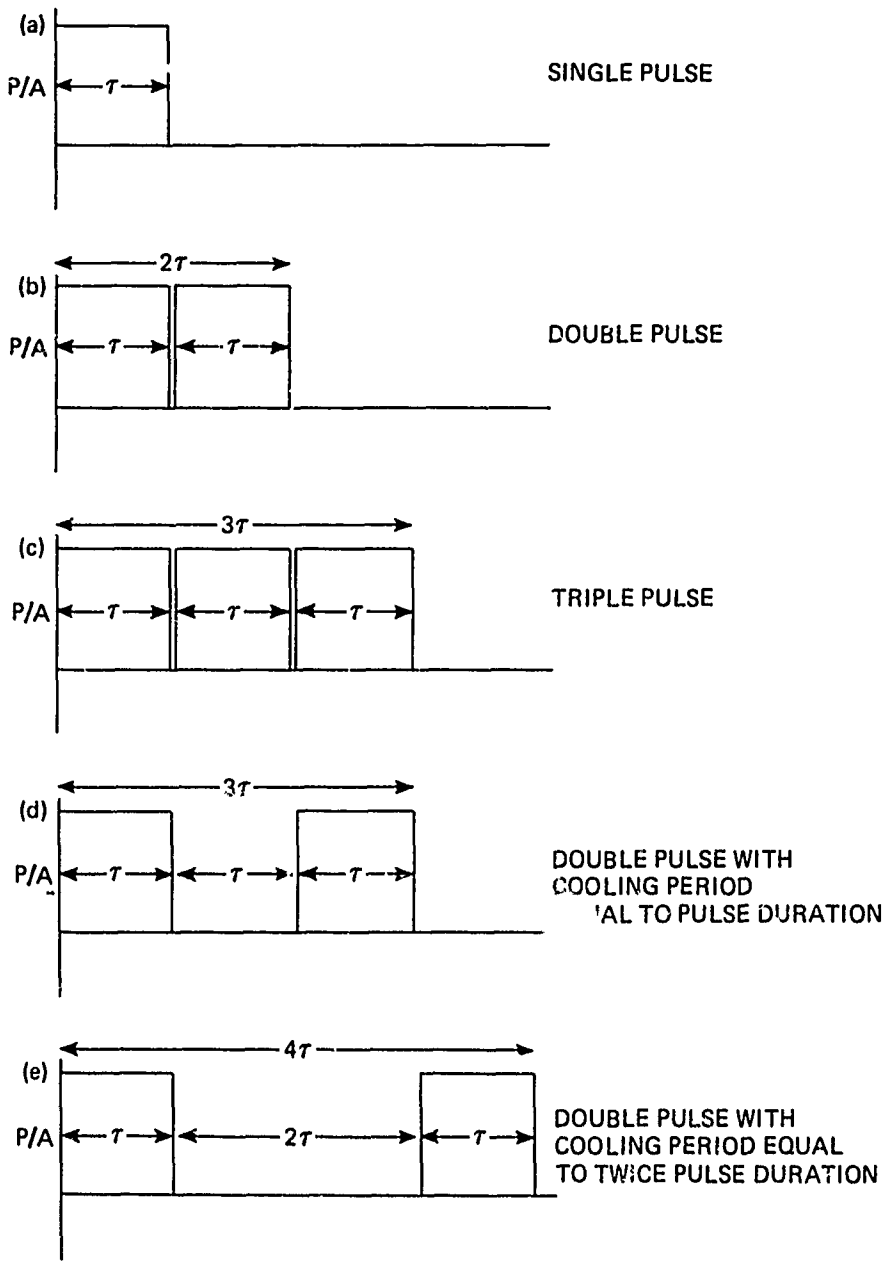

Figure 2.4

For all cases considered, we will assume an equal power level for the pulses and will plot the results in terms of the individual pulse duration τ.

SINGLE PULSE:

The failure levels for a single pulse were previously calculated from equation 1,

$$\frac{P}{A} = \sqrt{\pi\kappa\rho C_p}\,[T_m - T_i]t^{-1/2} \qquad (1)$$

where P is the power; A, the junction area; κ, the thermal conductivity; ρ, the density; C_p, the specific heat; T_m, the failure temperature; T_i, the initial temperature; and t, the time. For the cases where the failure temperature was assumed to be the melting temperature and (a) melting occurs over the entire junction and (b) melting occurs in local hot spots of one-tenth the total junction area, equation 1 becomes respectively:

$$\frac{P}{A} = 1810\ t^{-1/2} \qquad (2)$$

and

$$\frac{P}{A} = 181\ t^{-1/2}. \qquad (3)$$

These equations, along with the averaged curves** from actual experimental single-pulse failure data on diodes and transistors, are shown in Fig. 2.5.

MULTIPLE PULSE:

For multiple pulses, the worst case (lowest failure level) occurs when there is essentially no time between pulses for cooling. This is the type of pulses we see in cases 3 and 4 of Fig. 2.3. For analysis purposes, we will simulate such waveforms by multiple square wave pulses as shown in Fig. 2.4 (b, c) for the double and triple pulse. The use of square pulses will give a slightly lower failure level than would actually occur for sinusodial waveforms.

** These averages change slightly as more devices are tested. The analysis is still valid and the curves are only shifted slightly in a linear manner depending on the averaged value.

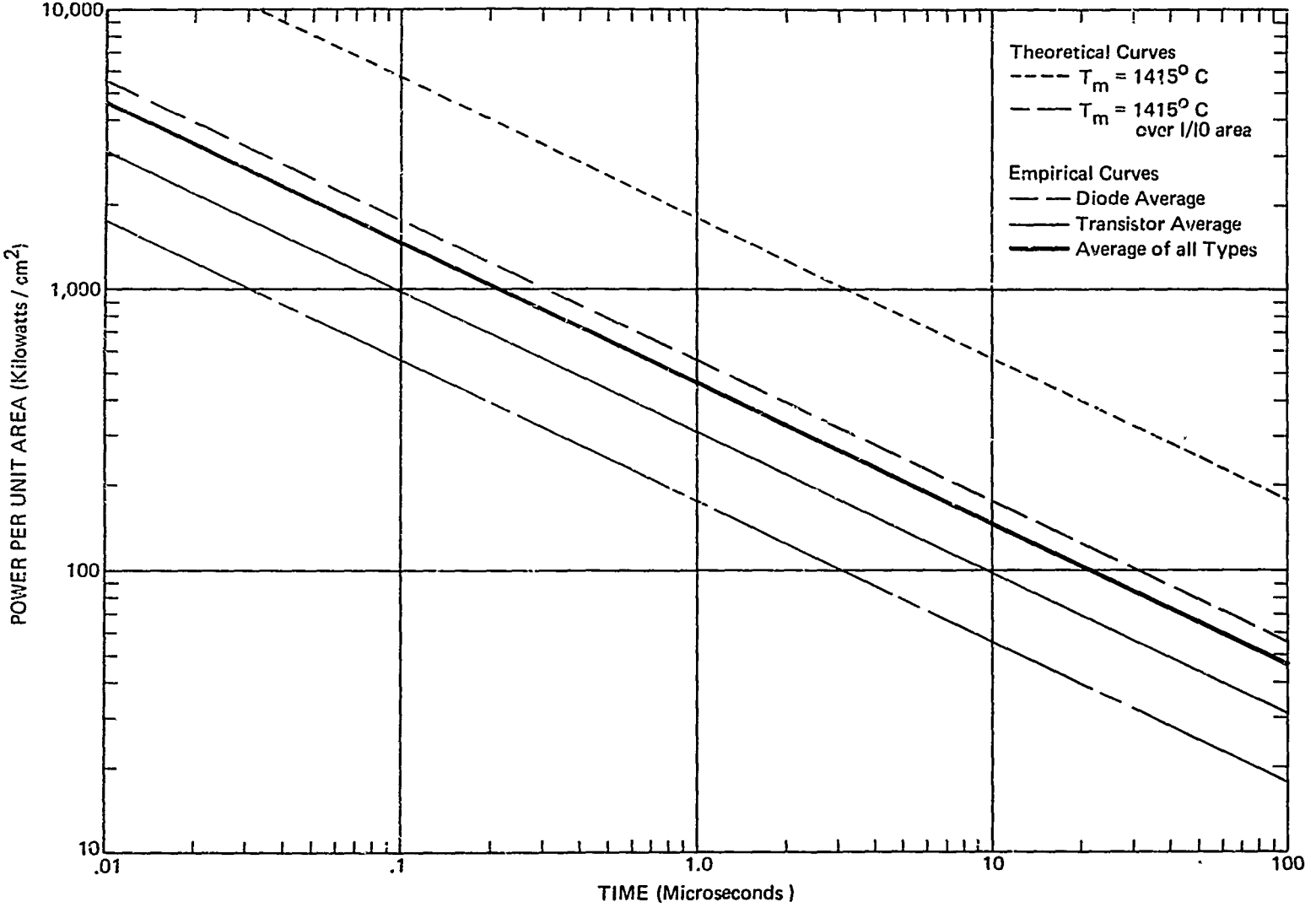
10,000
1,000
100
10
.01
.1
1.0
10
100
POWER PER UNIT AREA (Kilowatts / cm²)
TIME (Microseconds)
Theoretical Curves
T_m = 1415° C
T_m = 1415° C over 1/10 area
Empirical Curves
Diode Average
Transistor Average
Average of all Types

Figure 2.5

DOUBLE PULSE AND TRIPLE PULSE: (No cooling period)

Multiple pulses with no cooling between pulses can easily be calculated since the failure level is just the single pulse failure level for a single pulse whose duration is the sum of the multiple pulse durations. We can derive a general expression for the failure level for any number N of multiple pulses.

From equation 1, we have that the temperature is

$$[T_m - T_i] = \frac{\frac{P}{A}\, t^{1/2}}{\sqrt{\pi \kappa \rho C_p}}. \qquad (4)$$

For a single pulse of duration τ we have,

$$[T_m - T_i] = \frac{\frac{P}{A}\, \tau^{1/2}}{\sqrt{\pi \kappa \rho C_p}}. \qquad (5)$$

Then for a series of N multiple pulses each of duration τ and of equal power levels, we obtain

$$[T_m - T_i] = \frac{\frac{P}{A}\, (N\tau)^{1/2}}{\sqrt{\pi \kappa \rho C_p}} \qquad (6)$$

and that

$$\frac{P}{A} = N^{-1/2} \{\sqrt{\pi \kappa \rho C_p}\, [T_m - T_i]\, \tau^{-1/2}\} \qquad (7)$$

Equations 2 and 3 for multiple pulses are then

$$\frac{P}{A} = N^{-1/2}\, 1810\, t^{-1/2} \qquad (8)$$

and

$$\frac{P}{A} = N^{-1/2}\, 181\, t^{-1/2} \qquad (9)$$

The constant K for the equation

$$\frac{P}{A} = K\, t^{-1/2} \qquad (10)$$

for the theoretical estimated and for the averaged experimental data for transistors and diodes is given in Table I. The curves for single, double, and triple pulses for the above cases are given in Figs. 2.6 (Theoretical), 7 (Diodes), and 8 (Transistors).

TABLE I

Number of Pulses	Value of K of Equation 10			
	Theoretical	Curves	Diodes	Transistors
1	1810	181	560	310
2	1280	128	396	219
3	1045	105	323	179
4	905	91	280	155
5	809	81	250	139
6	739	74	229	127

Estimated failure levels for double and triple pulses for a 2N2222 transistor are shown in Fig. 2.9. These estimates are based on the actual experimental failure level for single pulses and on the above analysis.

DOUBLE PULSE: (with cooling period)

In order to make failure estimates for the power waveforms shown in Fig. 2.3 for cases 1 and 2, square wave pulses will again be assumed as shown in Fig. 2.4 (d, e).

Basically, the calculation of the failure levels will be done in three parts:

1. Calculation of the temperature distribution throughout the semiconductor due to the first pulse.
2. Calculation of the temperature distribution at the end of the cooling period.

ESTIMATED FAILURE CURVES FOR SEMICONDUCTOR JUNCTIONS

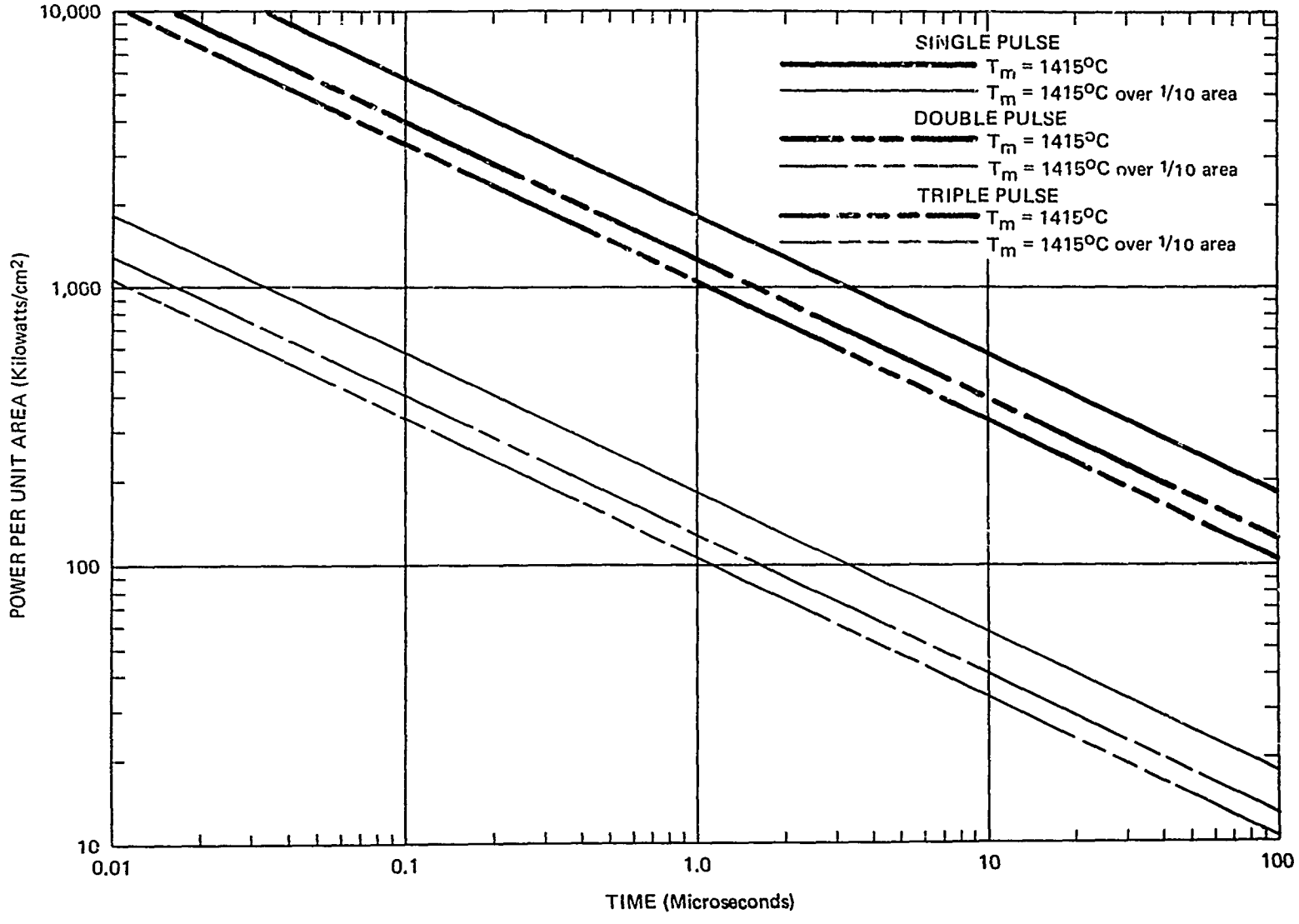

Figure 2.6

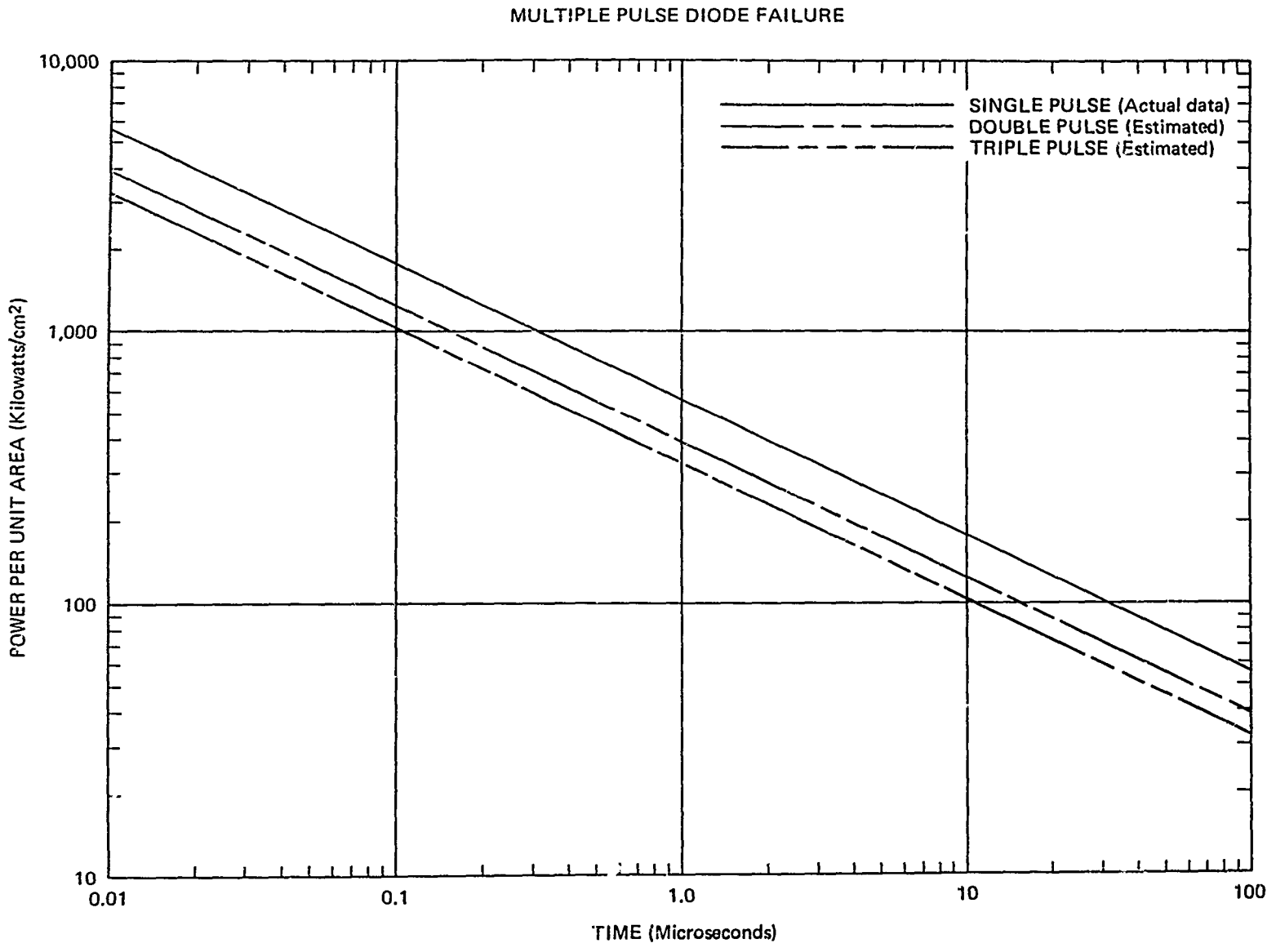
MULTIPLE PULSE DIODE FAILURE
10,000
1,000
100
10
POWER PER UNIT AREA (Kilowatts/cm²)
SINGLE PULSE (Actual data)
DOUBLE PULSE (Estimated)
TRIPLE PULSE (Estimated)
0.01
0.1
1.0
10
100
TIME (Microseconds)

Figure 2.7

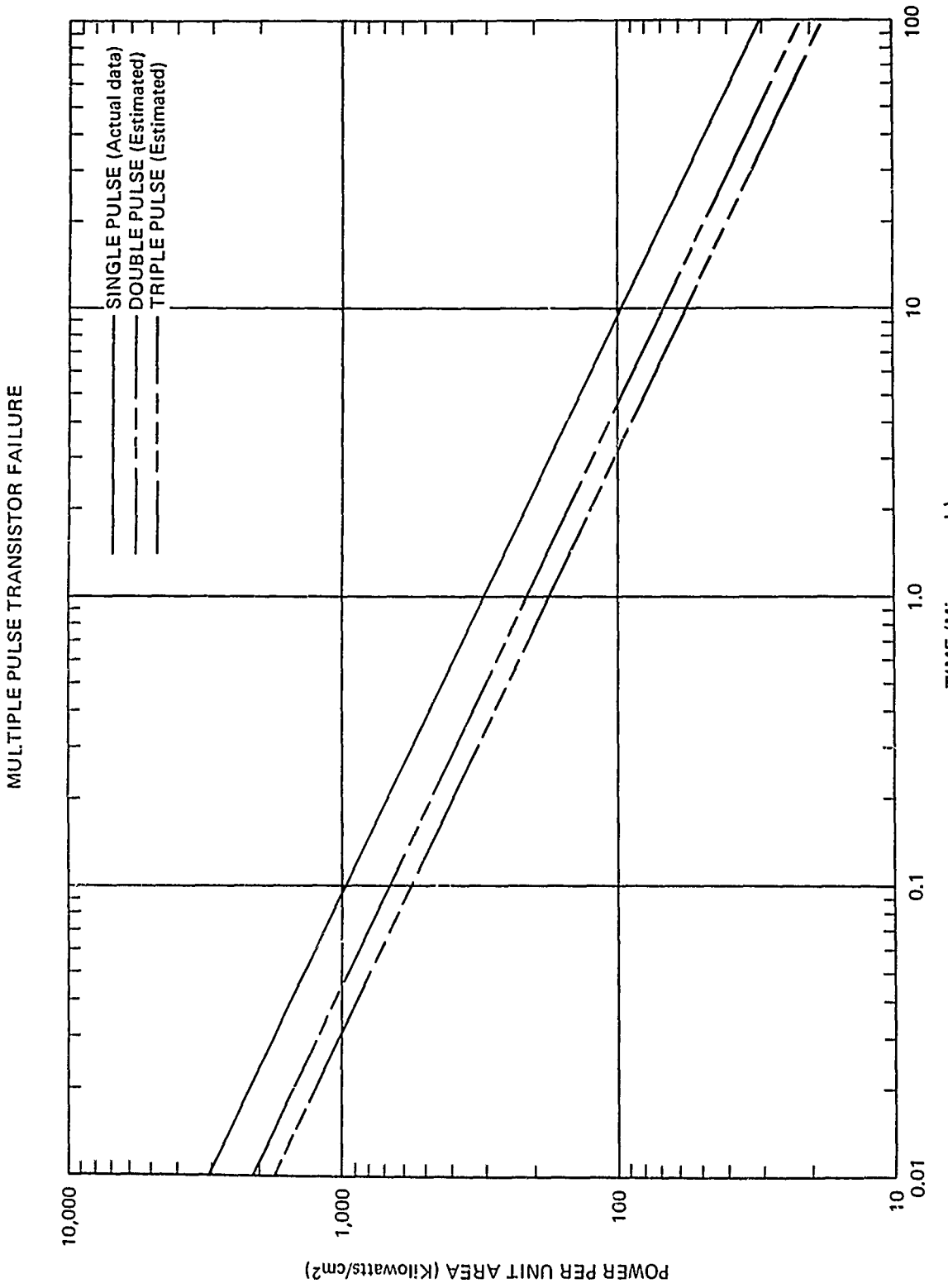
MULTIPLE PULSE TRANSISTOR FAILURE
SINGLE PULSE (Actual data)
DOUBLE PULSE (Estimated)
TRIPLE PULSE (Estimated)
POWER PER UNIT AREA (Kilowatts/cm2)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

Figure 2.8

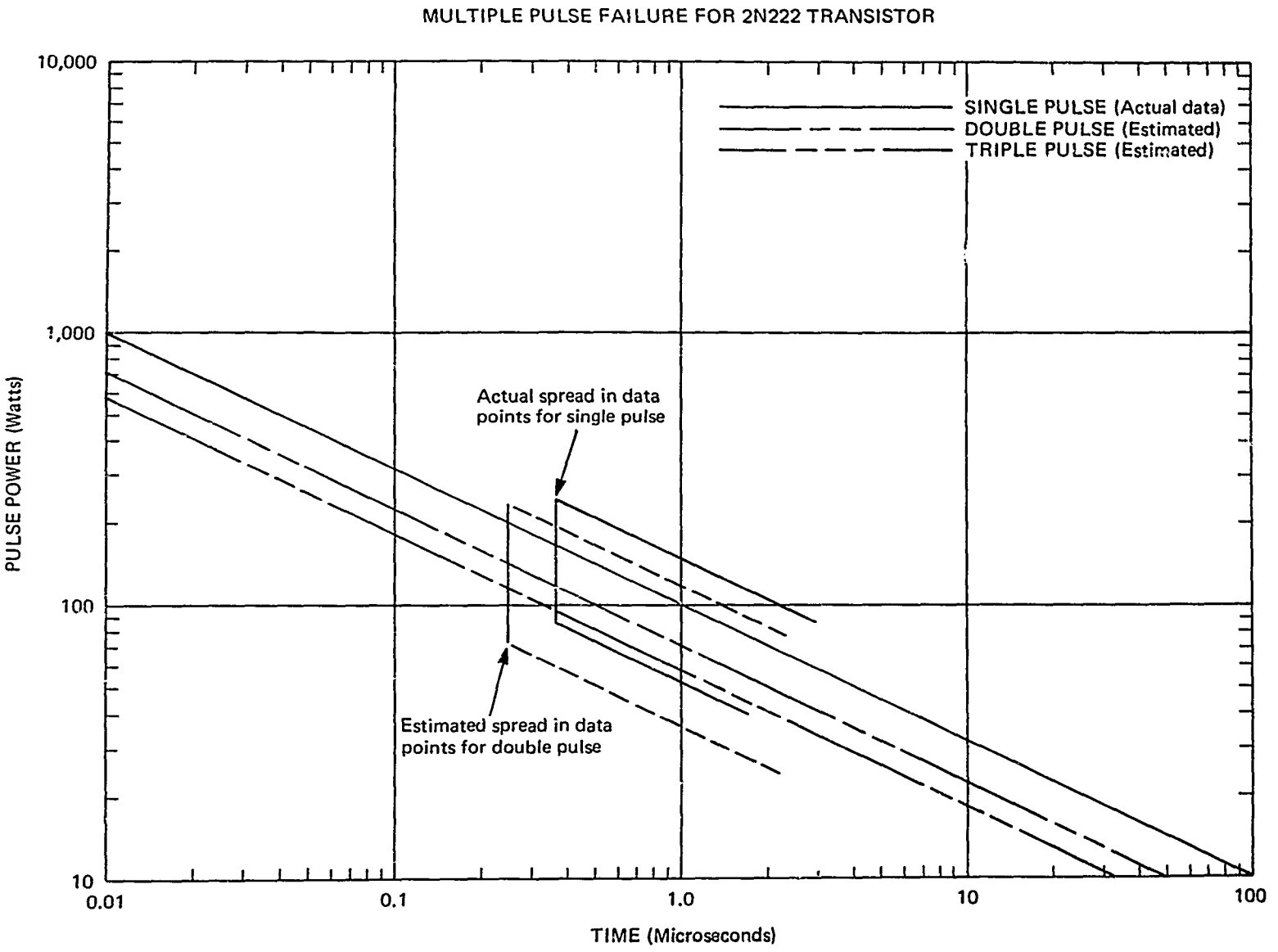
MULTIPLE PULSE FAILURE FOR 2N222 TRANSISTOR
SINGLE PULSE (Actual data)
DOUBLE PULSE (Estimated)
TRIPLE PULSE (Estimated)
Actual spread in data points for single pulse
Estimated spread in data points for double pulse
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

Figure 2.9

3. Calculation of the temperature at the junction due to the second pulse.

A. First Pulse Heating

The equation for the temperature divided by the power density is given by

$$\frac{T}{\frac{P}{A}} = \frac{t^{1/2}}{\sqrt{\pi\kappa\rho C_p}} e^{\frac{-x^2}{4\kappa\rho/C_p}} - \frac{|x|}{2} \operatorname{erfc} \frac{|x|}{2\sqrt{\kappa t/(\rho C_p)}}. \qquad (11)$$

A plot of the relative temperature versus distance from the junction for various pulse durations is shown in Fig. 2.10. The distance at which the temperature is down by 1/e from the junction temperature is marked.

B. Temperature After Cooling

A good approximation to the cooling can be found by using the equation

$$T = \frac{T_o}{2} \left\{ \operatorname{erf} \frac{a-x}{2\sqrt{\kappa t/(\rho C_p)}} + \operatorname{erf} \frac{a+x}{2\sqrt{\kappa t/(\rho C_p)}} \right\}. \qquad (12)$$

The above equation is valid for the case where the region $-a < x < a$ is initially at constant temperature T_o and the region $|x| > a$ is initially at zero.

From the temperature distribution of Part A (Fig. 2.10), we will estimate a value for 'a' for various pulse durations and calculate the normalized temperature distribution for various cooling durations. Table II gives the values of 'a' chosen for various heating-pulse durations.

RELATIVE TEMPERATURE OF SEMICONDUCTOR REGION FOR
VARIOUS HEATING–PULSE DURATIONS

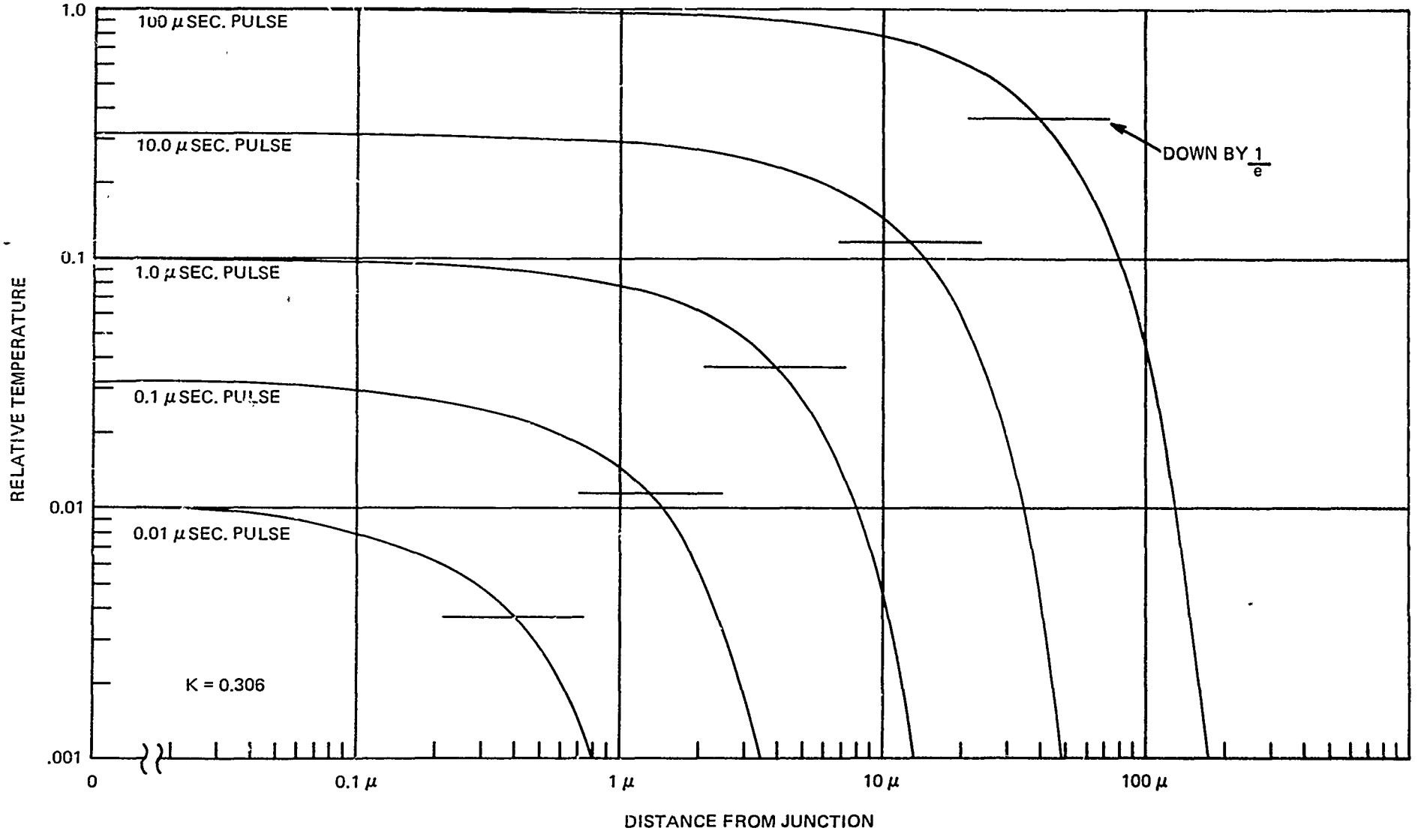

Figure 2.10

TABLE II	
Pulse Length (Microseconds)	a (Microns)
0.01	0.4
0.10	1.0
1.00	4.0
10.00	10.0
100.00	400.0

Figures 2.11, 2.12, and 2.13 are plots of the normalized temperature versus distance from the junction for various cooling times. The plots are for initialized heating due to 0.1, 1.0, and 10.0 microsecond pulses respectively.

C. Second Pulse Heating

Finally now we need to calculate the temperature rise due to the second pulse. Because th temperature of the device is no longer a constant throughout the device, we can no longer use the equation of Part A to calculate the temperature. In order to do this exactly, one needs to go back to the original heating equation and derive a new expression using a continuous plane source at the junction and include the actual temperature distribution as found in Part B. However, a reasonable estimate of the temperature due to the second pulse may be found by using equation 4 with a time duration equal to the actual pulse duration plus an "effective time" of the first pulse and cooling period. This "effective time" will be equal to the time required to heat the material to the temperature after the cooling period due to a power level of the first and second pulses. First, we need to derive the expression for $t_{effective}$, and then find the equation for the failure level due to both pulses. We will use f_c to denote the cooling factor at the junction as found from Figs. 11 to 13.

TEMPERATURE OF SEMICONDUCTOR REGION FOR VARIOUS COOLING TIMES

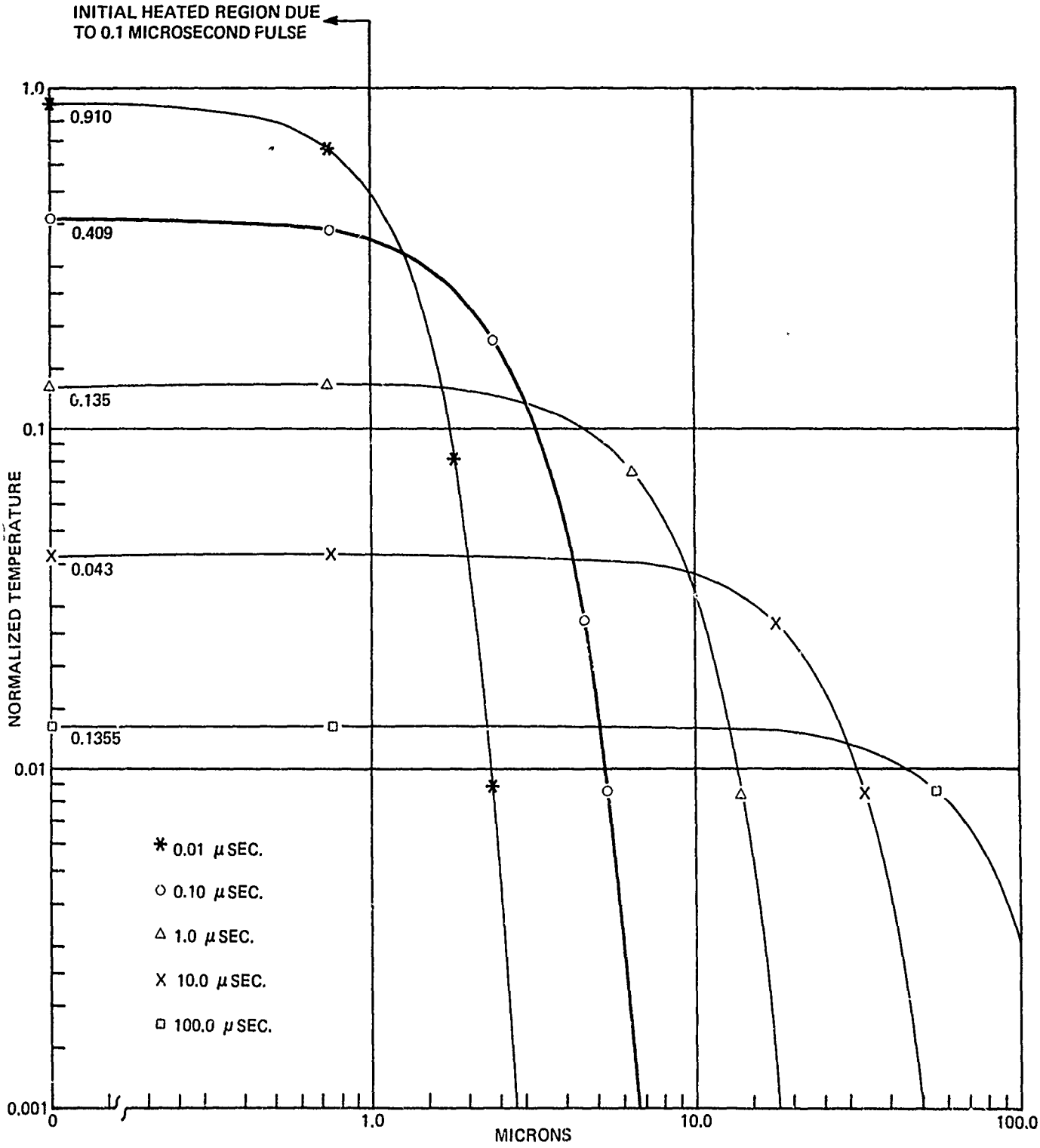

Figure 2.11

TEMPERATURE OF SEMICONDUCTOR REGION FOR VARIOUS COOLING TIMES

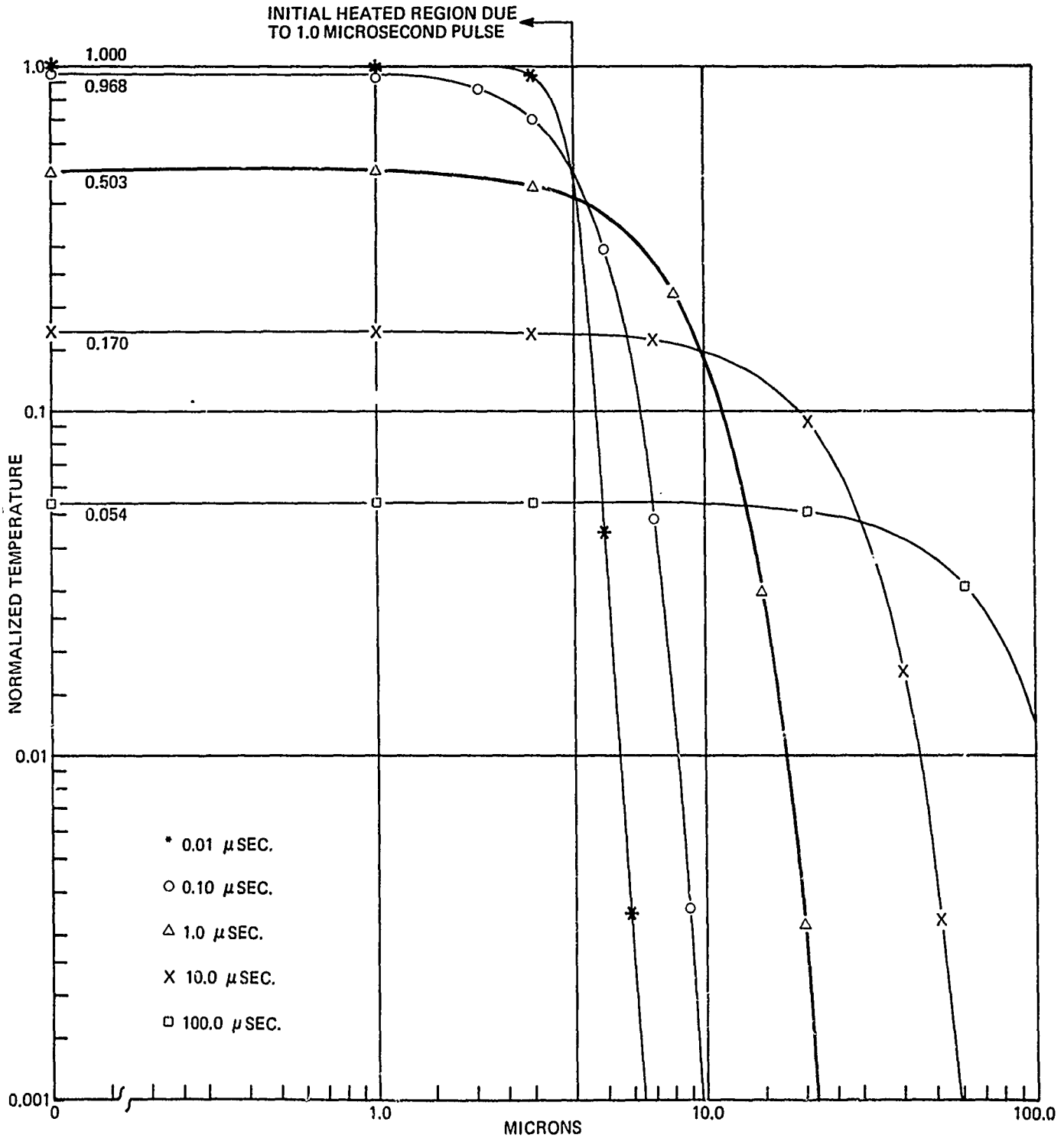

Figure 2.12

TEMPERATURE OF SEMICONDUCTOR REGION FOR VARIOUS COOLING TIMES

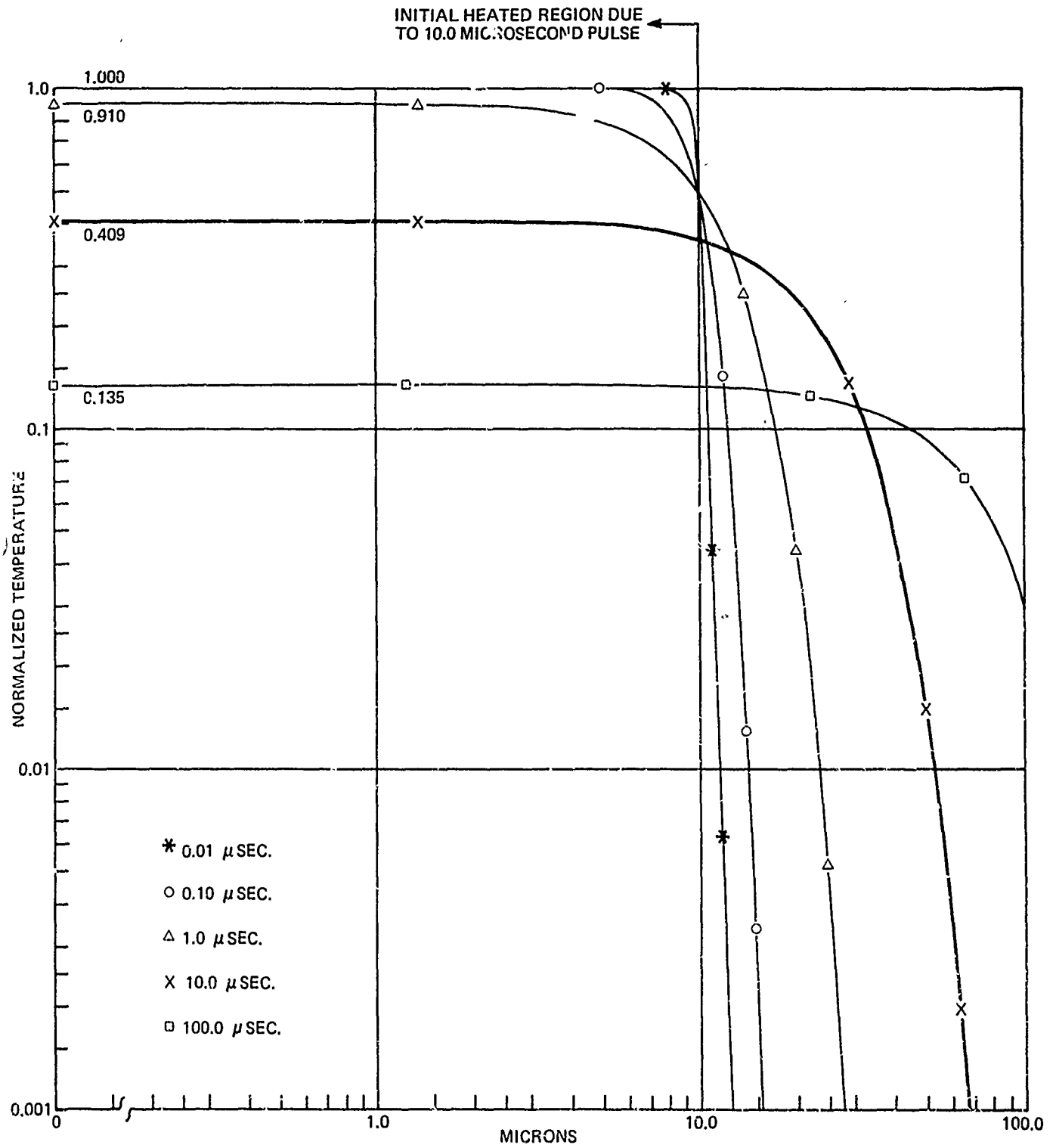

Figure 2.13

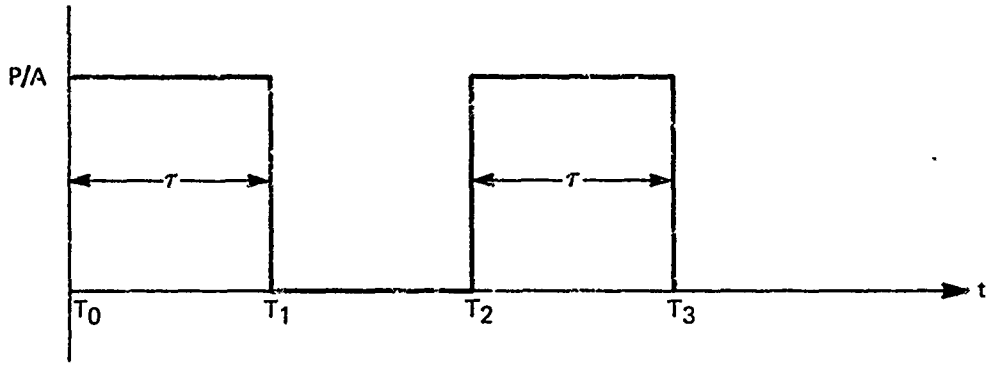

Figure 2.14

Using equation 4, we can write the equations for the various temperatures as shown in Fig. 14 as

$$[T_1-T_o] = \frac{P}{A} K \tau^{1/2}, \tag{13}$$

$$[T_2-T_o] = \frac{P}{A} K t_{eff}^{1/2}, \tag{14}$$

and

$$[T_3-T_o] = \frac{P}{A} K t_3^{1/2}. \tag{15}$$

where

$$t_3 \equiv \tau + t_{eff} \quad \text{and} \quad K \equiv (\pi\kappa\rho C_p)^{-1/2} \tag{16}$$

Also

$$T_2 = f_c [T_1-T_o] + T_o \tag{17}$$

Equation 14 then becomes

$$\{f_c [T_1-T_o] + T_o-T_o\} = \frac{P}{A} K t_{eff}^{1/2} \tag{18}$$

Solving for t_{eff}, we have

$$t_{eff} = \frac{f_c^2 [T_1 - T_o]^2}{(\frac{P}{A} K)^2} . \tag{19}$$

From equation 13

$$T_1 = \frac{P}{A} k \tau^{1/2} + T_o \tag{20}$$

Then (19) becomes

$$t_{eff} = \frac{f_c^2 [\frac{P}{A} K \tau^{1/2} + T_o - T_o]^2}{(\frac{P}{A} K)^2} = f_c^2 \tau. \tag{21}$$

Now using equations 15, 16, and 21 with $T_3 = T_m$, we have

$$[T_m - T_o] = \frac{P}{A} K (\tau + t_{eff})^{1/2} = \frac{P}{A} K (\tau + f_c^2 \tau)^{1/2} \tag{22}$$

Then

$$\frac{P}{A} = \frac{\sqrt{\pi \kappa \rho C_p} [T_m - T_o] \tau^{-1/2}}{(1 + f_c^2)^{1/2}}. \tag{23}$$

From equation 23, we can now calculate our failure levels for a double pulse with a cooling time between pulses. Note that for no cooling, $f_c = 1$ and $(1 + f_c^2)^{1/2} = \sqrt{2}$, which makes equation 23 reduce exactly to equation 7, which we had derived previously. An example of how the cooling period affects the failure level is shown for the transistor case in Fig. 15 with the calculated values given in Table III. The 0.1 and 10 microsecond points differ slightly relative to the 1 microsecond point because the length of the heated region was chosen at the distance where the temperature was down by 36.8% (i.e., $\frac{1}{e}$) for the 1.0 microsecond pulse and at the distance where the temperature was down by 46.8% for the 0.1 and 10.0 microsecond points.

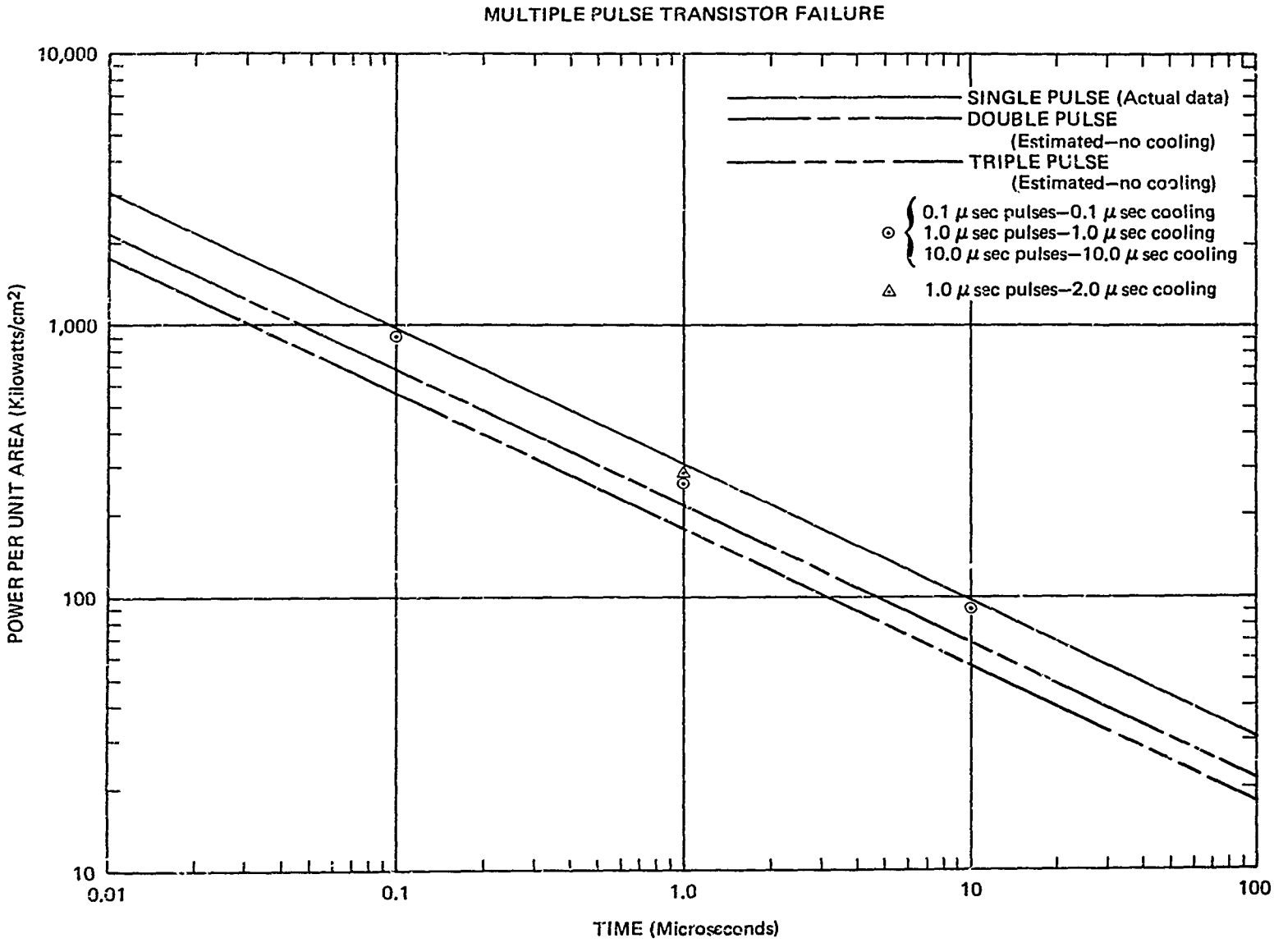
MULTIPLE PULSE TRANSISTOR FAILURE
10,000
1,000
100
10
0.01
0.1
1.0
10
100
POWER PER UNIT AREA (Kilowatts/cm²)
TIME (Microseconds)
SINGLE PULSE (Actual data)
DOUBLE PULSE
(Estimated—no cooling)
TRIPLE PULSE
(Estimated—no cooling)
0.1 μ sec pulses—0.1 μ sec cooling
1.0 μ sec pulses—1.0 μ sec cooling
10.0 μ sec pulses—10.0 μ sec cooling
1.0 μ sec pulses—2.0 μ sec cooling

Figure 2.15

TABLE III	
Double Pulse Failure	
Condition	Value of K of Eq. 10
1.0 microsecond pulses No cooling	219
1.0 microsecond pulses 1.0 microsecond cooling	277
1.0 microsecond pulses 2.0 microsecond cooling	291
0.1 microsecond pulses 0.1 microsecond cooling	907
10.0 microsecond pulses 10.0 microsecond cooling	90.7

DISCUSSION

Although we feel that the multiple pulse analysis discussed is generally valid, there may be some devices whose failure levels may differ from those predicted.

For large area diodes we have noted that pulses of long duration and large powers can be dissipated without damage until a certain power level - time duration is reached. If the power level is then raised slightly the device fails in very short times. We believe that this phenomena is due to the diode initially conducting over most of the junction area until a certain temperature and electric field gradient is reached. Then a small hot spot or breakdown occurs in a very localized region. When this occurs, a heavy current is channeled through the hot spot and the device quickly fails. What happens then when pulse trains as shown in Fig. 2.2 are applied to such a device? In this case, a steady power level and unidirectional voltage is not maintained. The lower power level and the change in voltage polarity as the voltage wave goes into

the second pulse may sufficiently change the conditions for breakdown and hot spot formation that the device might not fail as readily. On the other hand, a very rapid change in applied voltage polarity may result in some very high local field gradients in the junction and breakdown conditions might be enhanced. However, in either case, drastic deviations from the estimated failure levels are not expected.

Another precaution one should note is on cases 1 and 2, where we have assumed that reverse conduction does not occur. For small signals this is certainly true; however, for the power levels we are discussing, the first conduction pulse will cause very high junction temperatures. At such temperatures, the reverse voltage breakdown characteristic is drastically changed. Conduction may then actually occur during the reverse cycle. The momentary change in breakdown voltage cannot be noted from our single pulse experiments since the device has sufficient time to cool before a measurement can be made on the transistor curve tracer.

CONCLUSIONS

It is felt that the foregoing analysis shows that one does not expect drastic changes in the failure levels due to a series of several pulses. The general order of magnitude failure level still holds. Even for the worst case of assuming continuous power flow for the sum duration of all the pulses, the results are still of the same order of magnitude. Any cooling shifts the curves back toward the single pulse failure level. Also, as shown in Fig. 9, the estimated failure level for a triple pulse is actually still within the spread of experimental data points for a single pulse.

The worst case condition described by equation 7 is probably adequate to describe all multiple pulse conditions if one is only interested in an order of magnitude estimate of the failure level.

SECTION 3.

INTRODUCTION

I. Semi-Empirical Threshold Power Failure Equation

A final re-evaluation of test data for all the Pershing semiconductor damage tests produced the results shown in Tables I and II of this section. The significant numbers in these tables are listed under column heading $K^1(\text{watt-sec}^{1/2})$. These numbers allow semi-empirical threshold power failure levels to be obtained from the relation

$$P_{thres} = K^1 t^{-1/2}.$$

Threshold power failure levels will be obtained in watts when pulse widths, t, are expressed in seconds. This is the semi-empirical equation (based on the thermal failure model) which permits order of magnitude estimates of the failure level by adjusting the K^1 constant to best fit the data. Presented in this manner, the semiconductor damage results are in the proper form for circuit-response-to-transient analyses and further interpretation of the data is unnecessary.

II. Threshold Power Failure Levels for Devices When Damage is Achieved

The general experimental procedure to determine the threshold power failure level of semiconductor junctions consists of voltage pulsing the junction until failure occurs. "Failure" is arbitrarily defined to be a 15% reduction in transistor DC current gain (H_{FE}) or a similiar degradation in diode zener voltage. From this data, plots of power versus pulse duration are obtained. Based on these plottings, a semi-empirical threshold power failure curve is drawn. This curve reflects the reverse failure points, no failure points, and the uncertainty in the data for each point. The failure

curve is described by the equation

$$P = K^1 t^{-1/2}.$$

From the test results obtained, it can be predicted with a high degree of confidence that power levels an order of magnitude higher than those levels estimated by the threshold power failure equation will produce device failure; conversely, power levels an order of magnitude lower than those indicated by the equation will not cause device degradation.

III. Threshold Power Failure Levels for Devices When Damage is Not Achieved

Device failure for a number of large-area diodes and transistors was not possible within the limits of the BDM pulser. For these devices, threshold power damage levels were estimated from junction areas and the "standard" P/A versus time curves shown in Figure 3.1. These curves are defined by $P/A = K^1/A\ t^{-1/2}$, where the constant, K^1/A, represents the average value obtained from diodes or transistors which were damaged. The resulting K^1/A constants are

$$\frac{K^1}{A} = (0.554 \times 10^3)\ \text{watt-sec}^{1/2}/\text{cm}^2 \qquad \text{for diodes}$$

$$\frac{K^1}{A} = (0.47 \times 10^3)\ \frac{\text{watt-sec}^{1/2}}{\text{cm}^2} \qquad \text{for transistors}$$

Multiplying the appropriate average K^1/A value above by the junction area of an undamaged device yields an "estimated" K^1. Having this estimated K^1 value, a threshold power failure curve can be drawn for the diode or

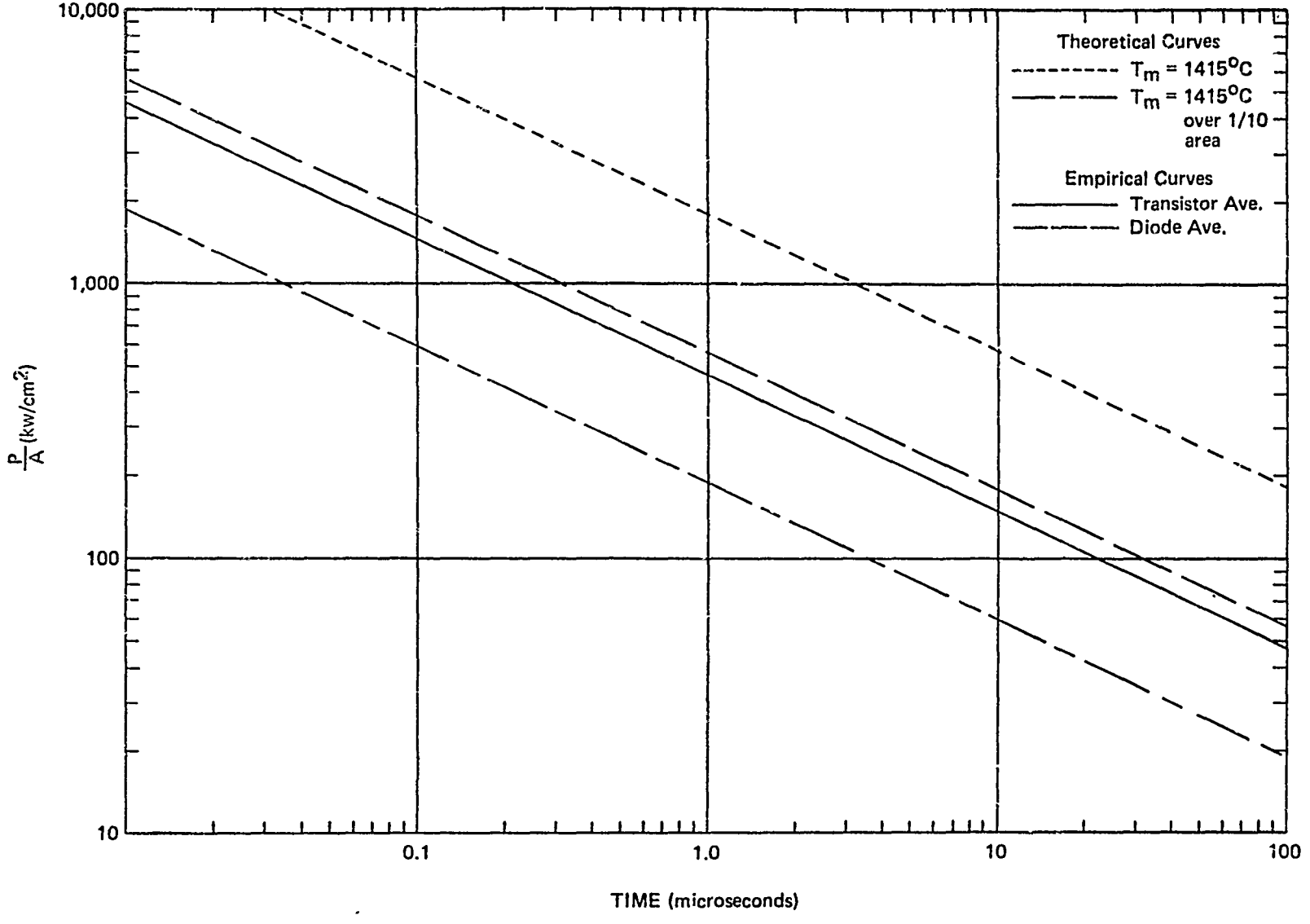

FIGURE 3.1 Standard $\frac{P}{A}$ vs. Time Curves.

transistor not damaged.

A slight departure from the prediction of the threshold power failure equation was denoted for the large area devices. As a result, it is anticipated that a higher power failure level is estimated by this equation for those undamaged, large area devices. This undetermined error is especially true for components having junction areas measuring in tenths of square centimeters.

IV. Device Damage Plots

Plots of power versus pulse duration for each device tested are contained in this section. The solid line on the plot represents the threshold power failure curve; the dotted line drawn on the plot represents the estimated threshold power failure curve defined in Paragraph III.

INDEX TO THRESHOLD POWER FAILURE CURVES

1. Diode and SCR Reports

1N751A (10627745)	3.30
1N752A	3.31
1N753A (5960-842-3525)	3.32
1N763-2 (10587417-3)	3.33
1N816 (10587418-1)	3.34
1N823 (10588877)	3.35
1N933J (5960-842-3525)	3.36
1N939A (10607918-1)	3.37
1N967B	3.38
1N981B	3.39
1N1095 (816 B520 P5)	3.23
1N1342A (R051060113)	3.40
1N1585 (998A562G11)	3.41
1N1770A (10627719-1)	3.42
1N1783 (10627724-1)	3.43
1N2929A (11040282-1)	3.44
1N3016B	3.45
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1N4817 (R051074657)	3.46
1N4820 (R051074768)	3.46
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G100 (MIS17007/1-1)	3.48
G129 (10611651-1)	3.49
MC357 (MIS17197/1-1)	3.50

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2N498 (10630123-1)	3.85
2N526	2.86
2N576A	3.88
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2N1039	3.103
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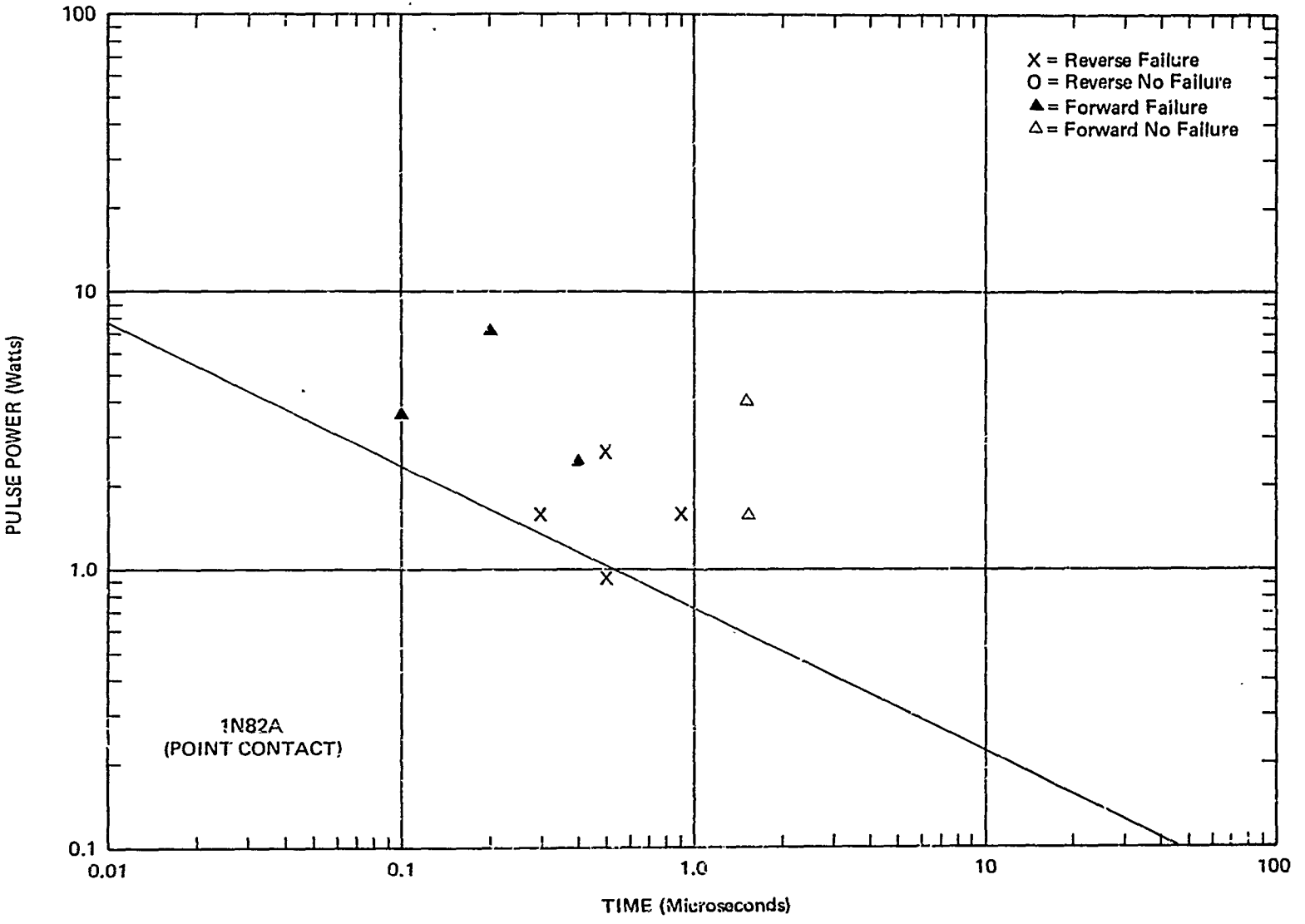
2N1115	3.106
2N1116A (10630124)	3.107
2N1132 (10630132-1)	3.108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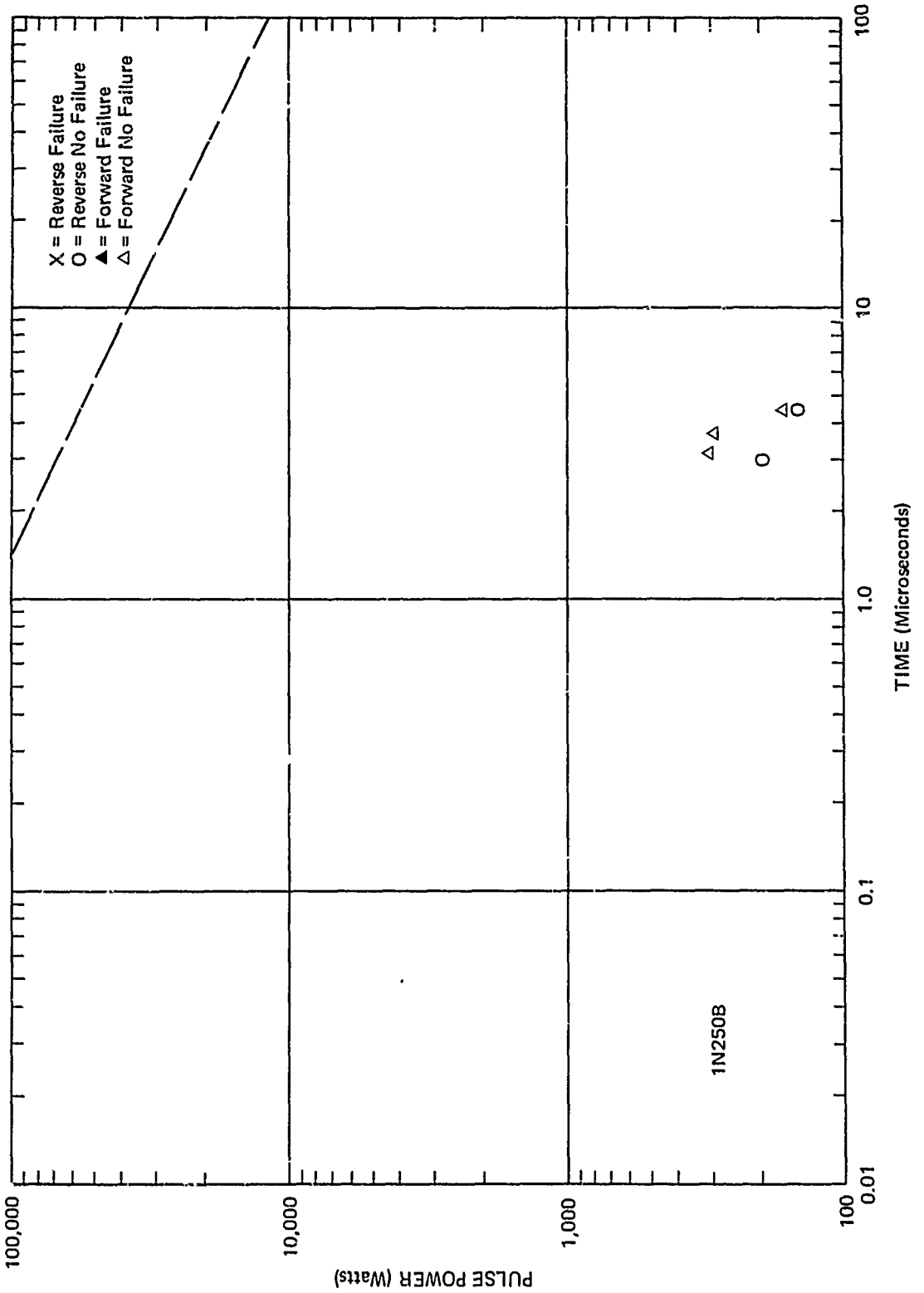
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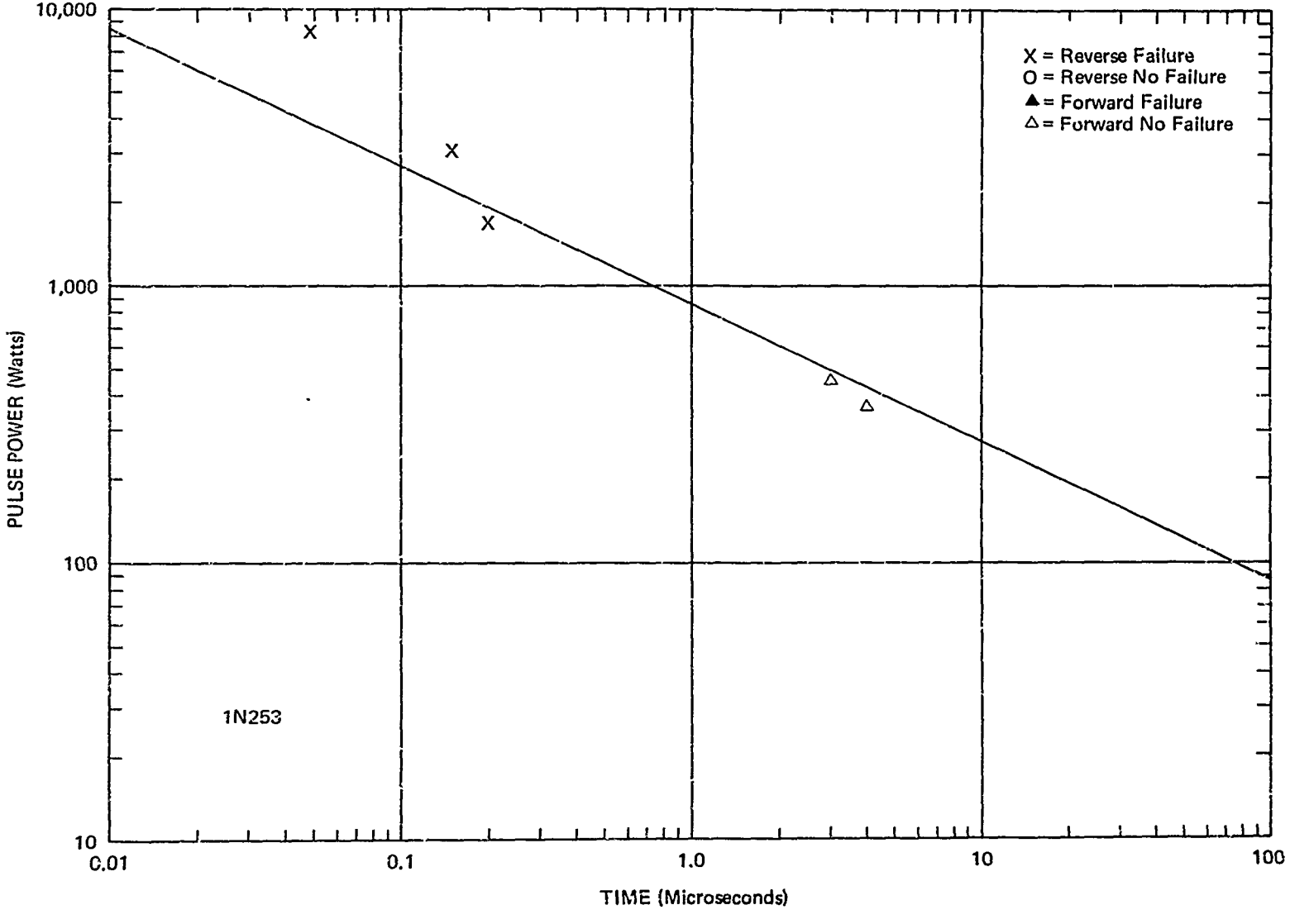
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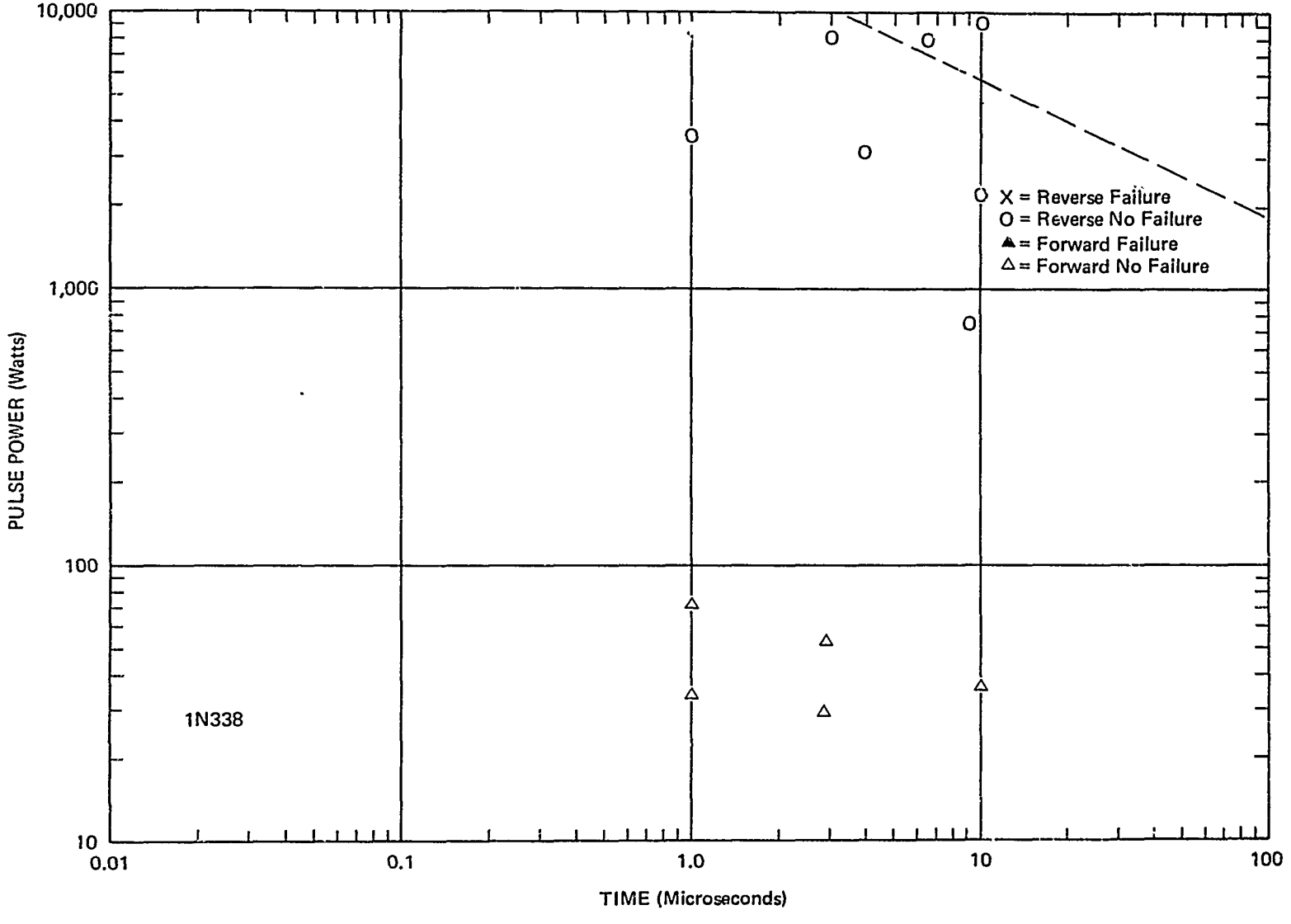
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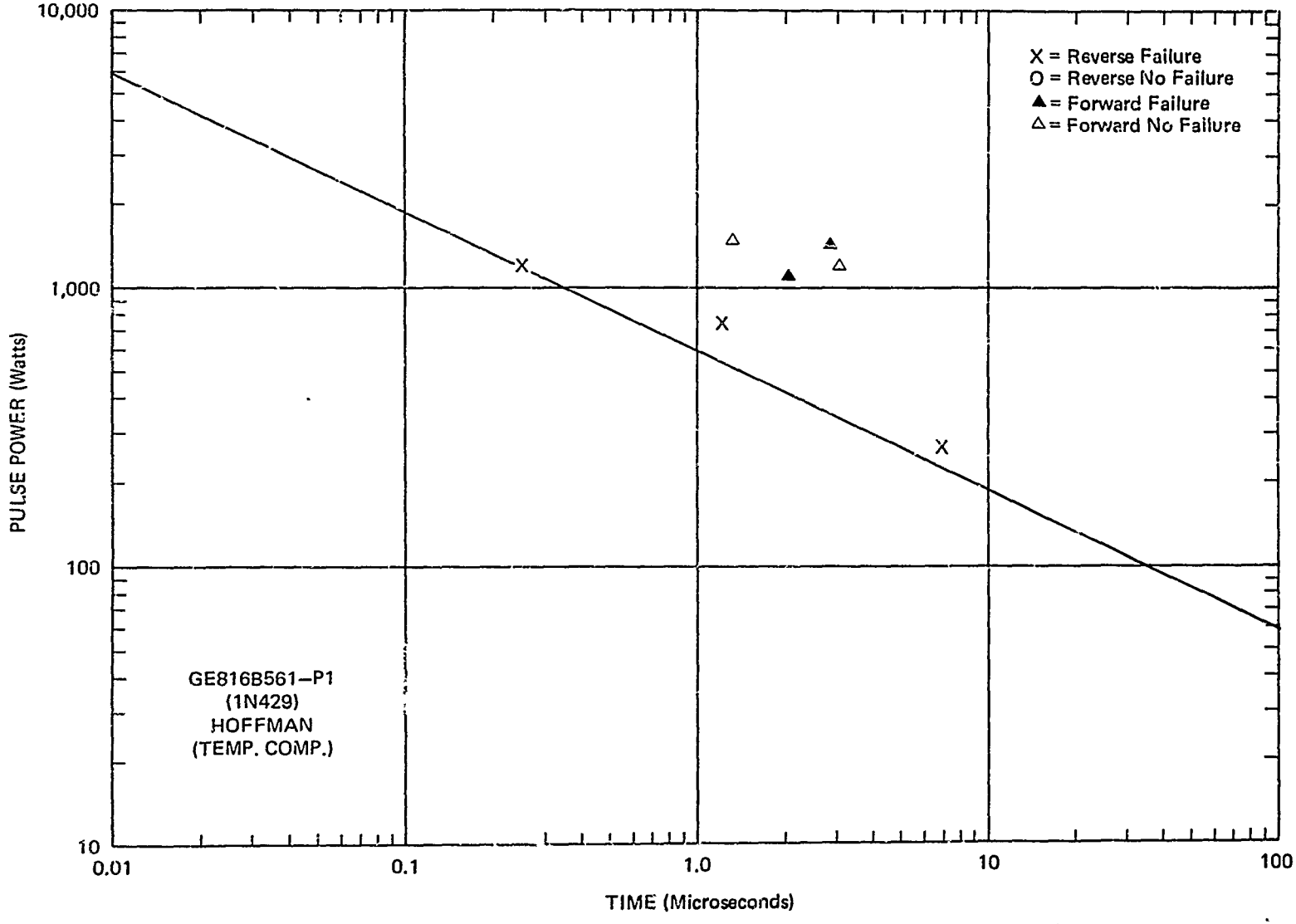
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HOFFMAN
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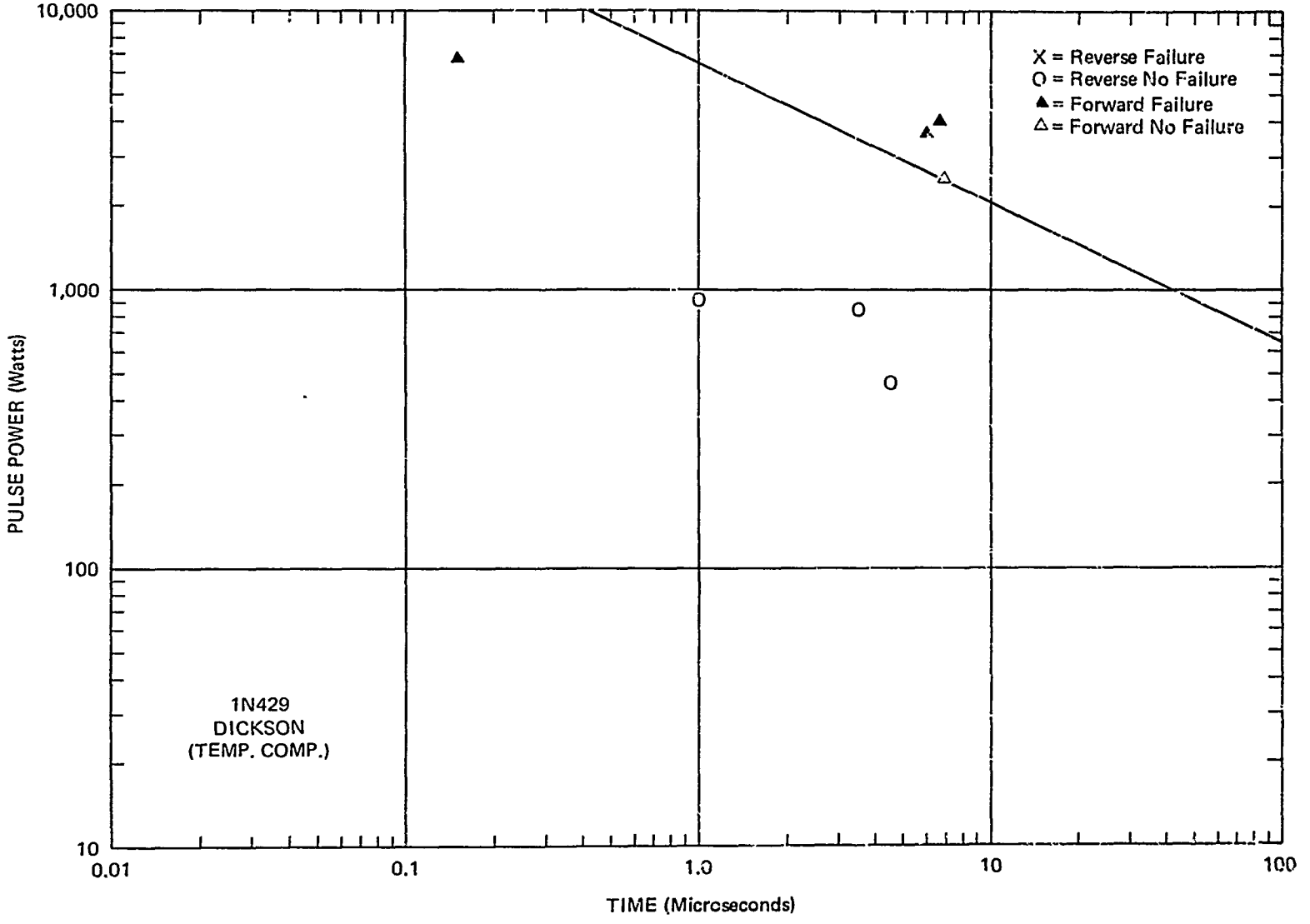
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DICKSON
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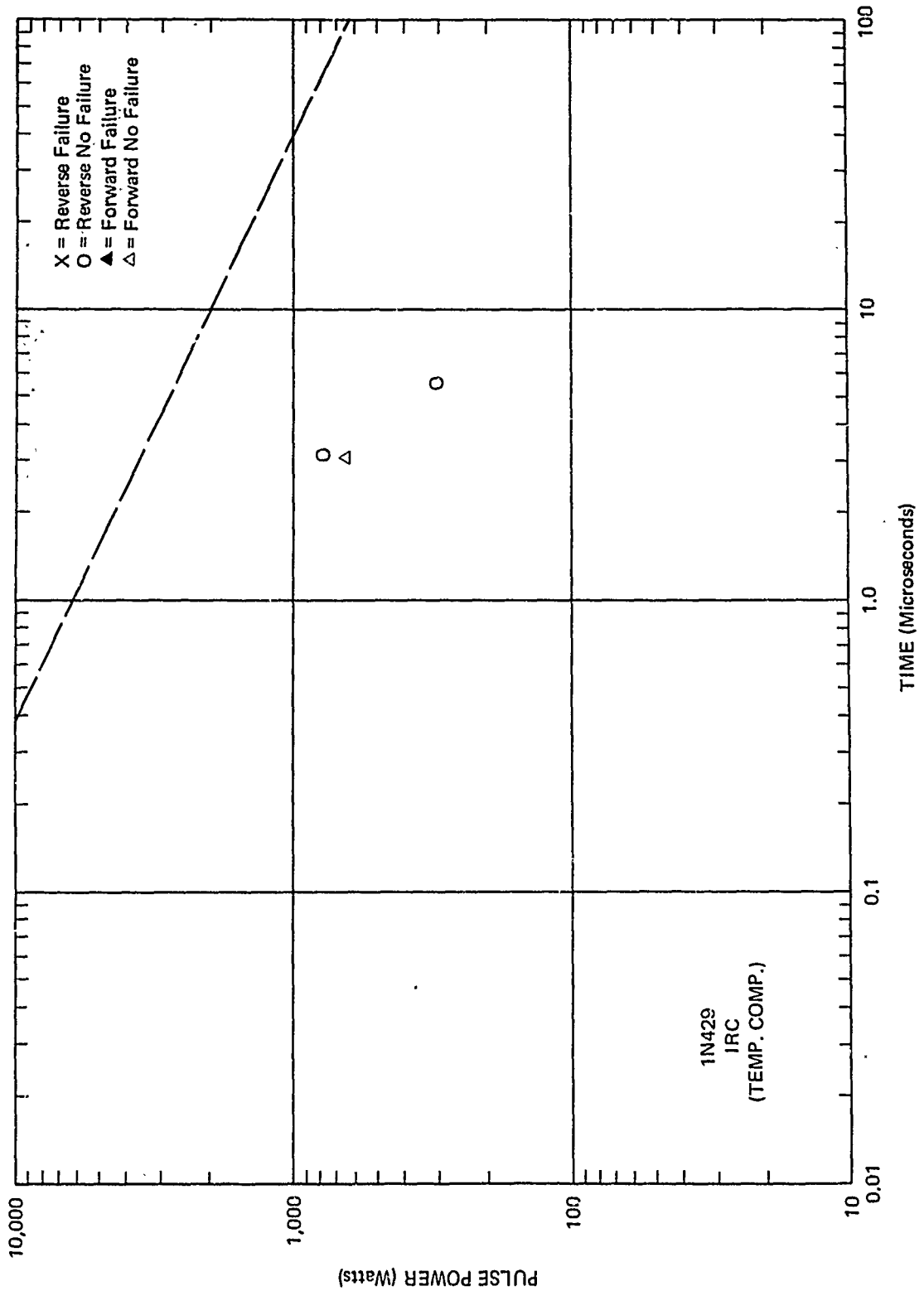
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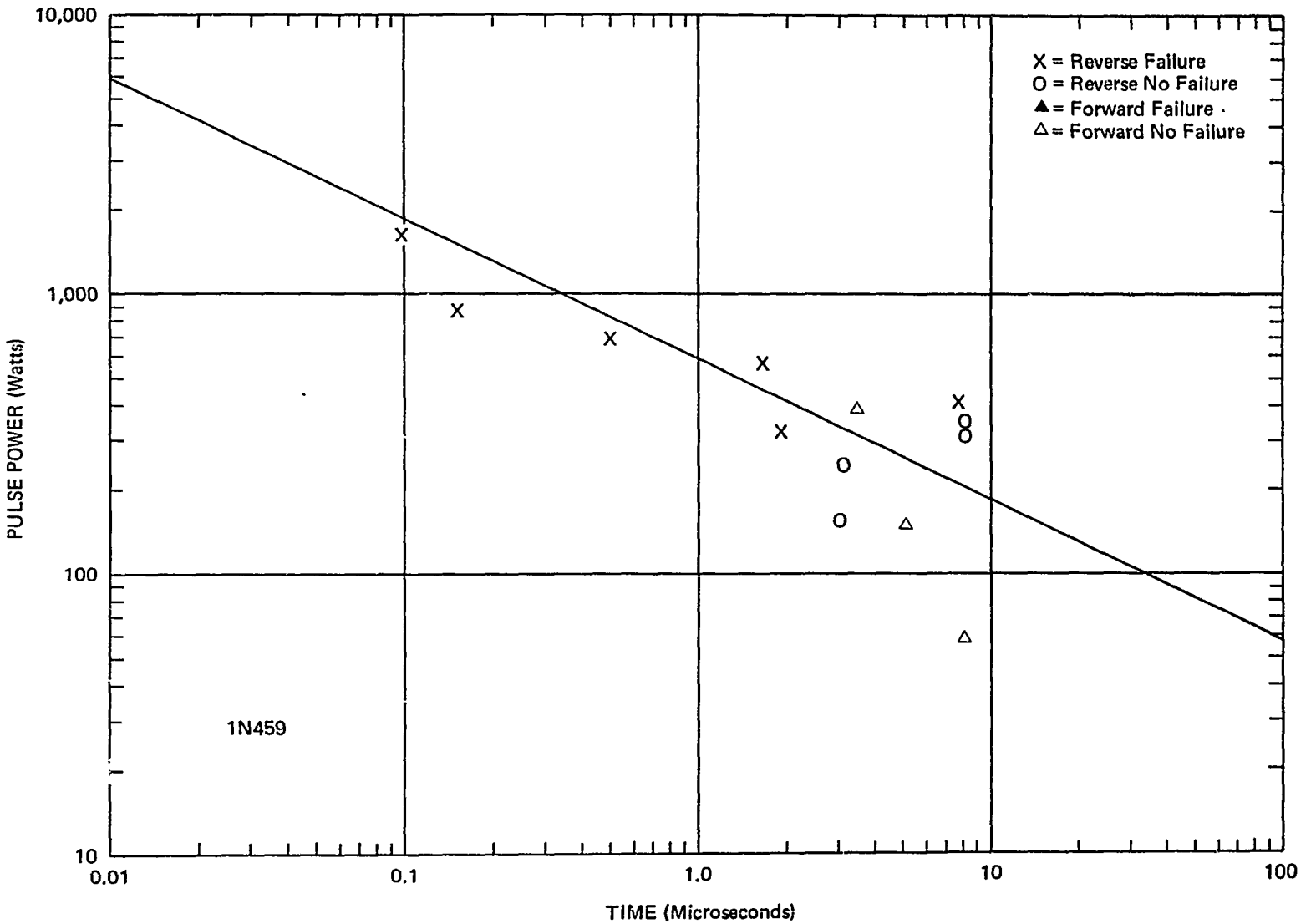
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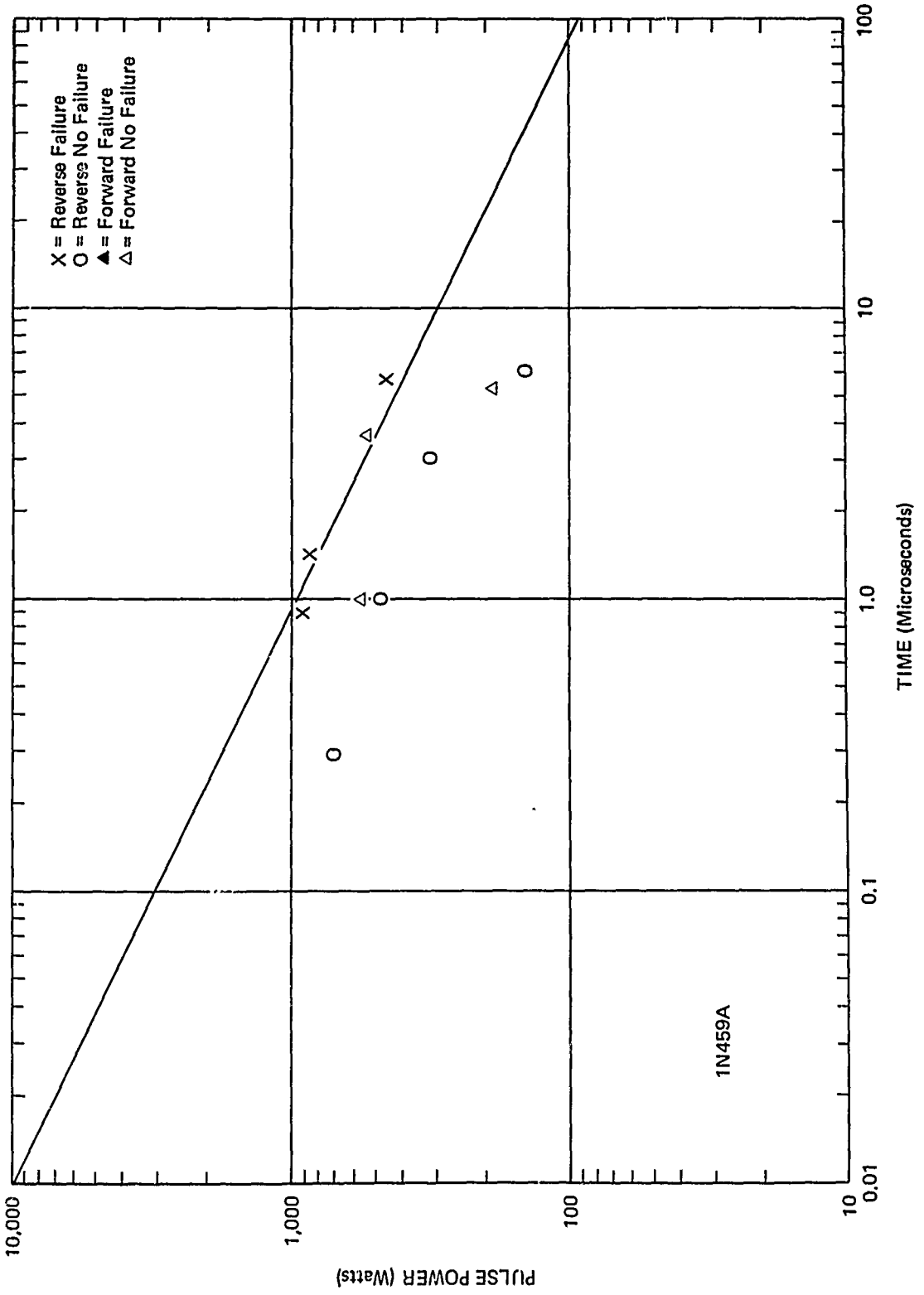
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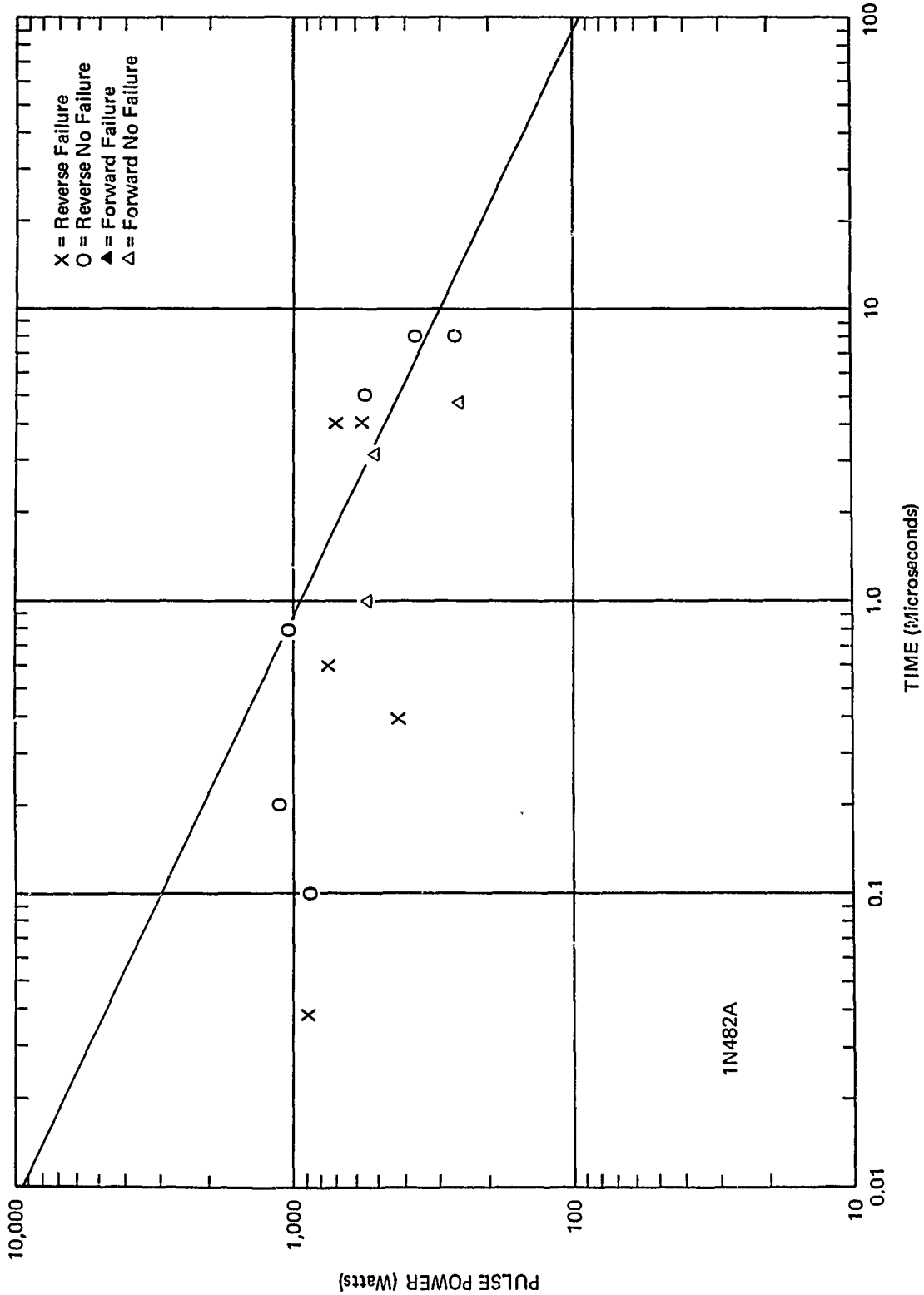
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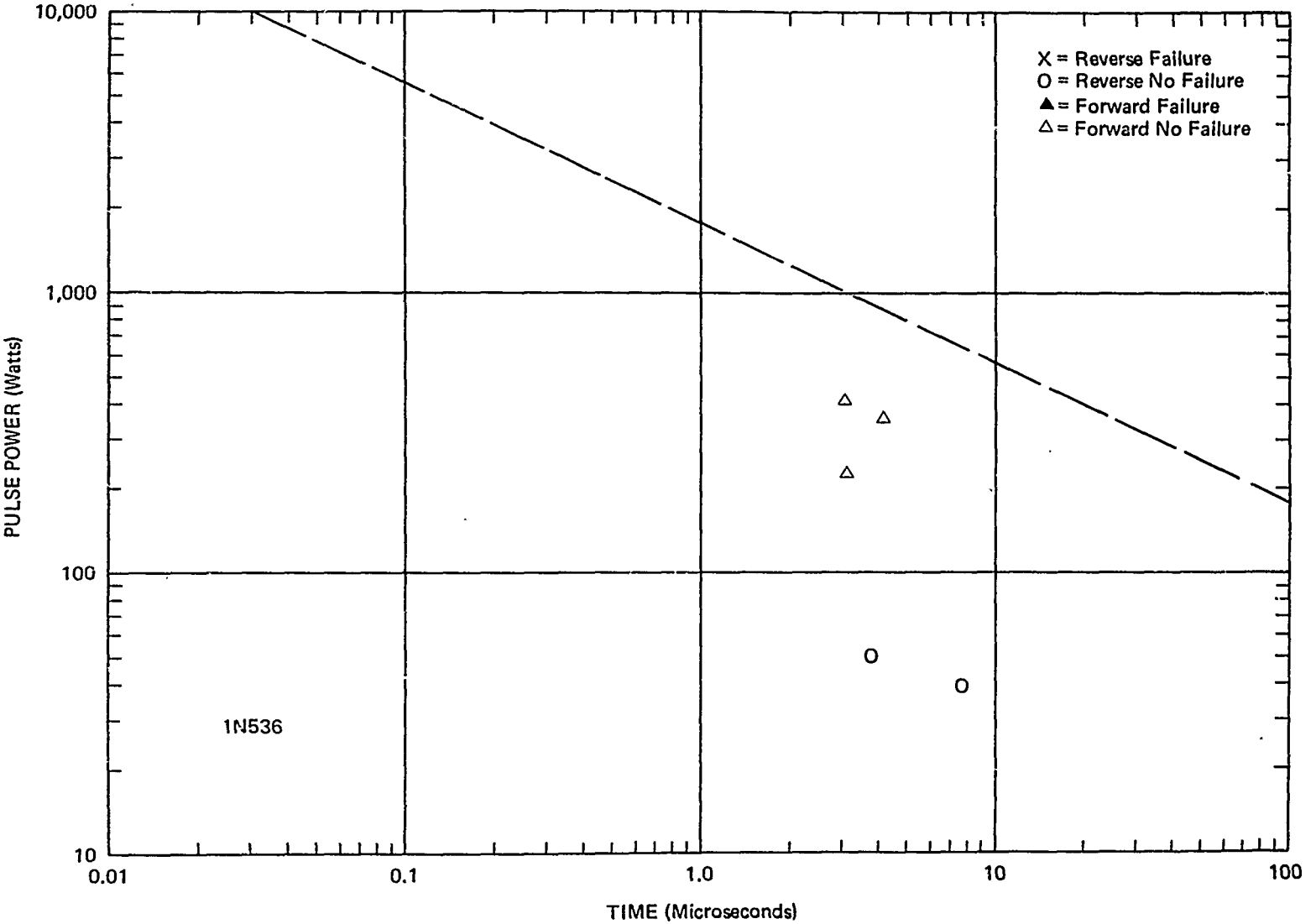
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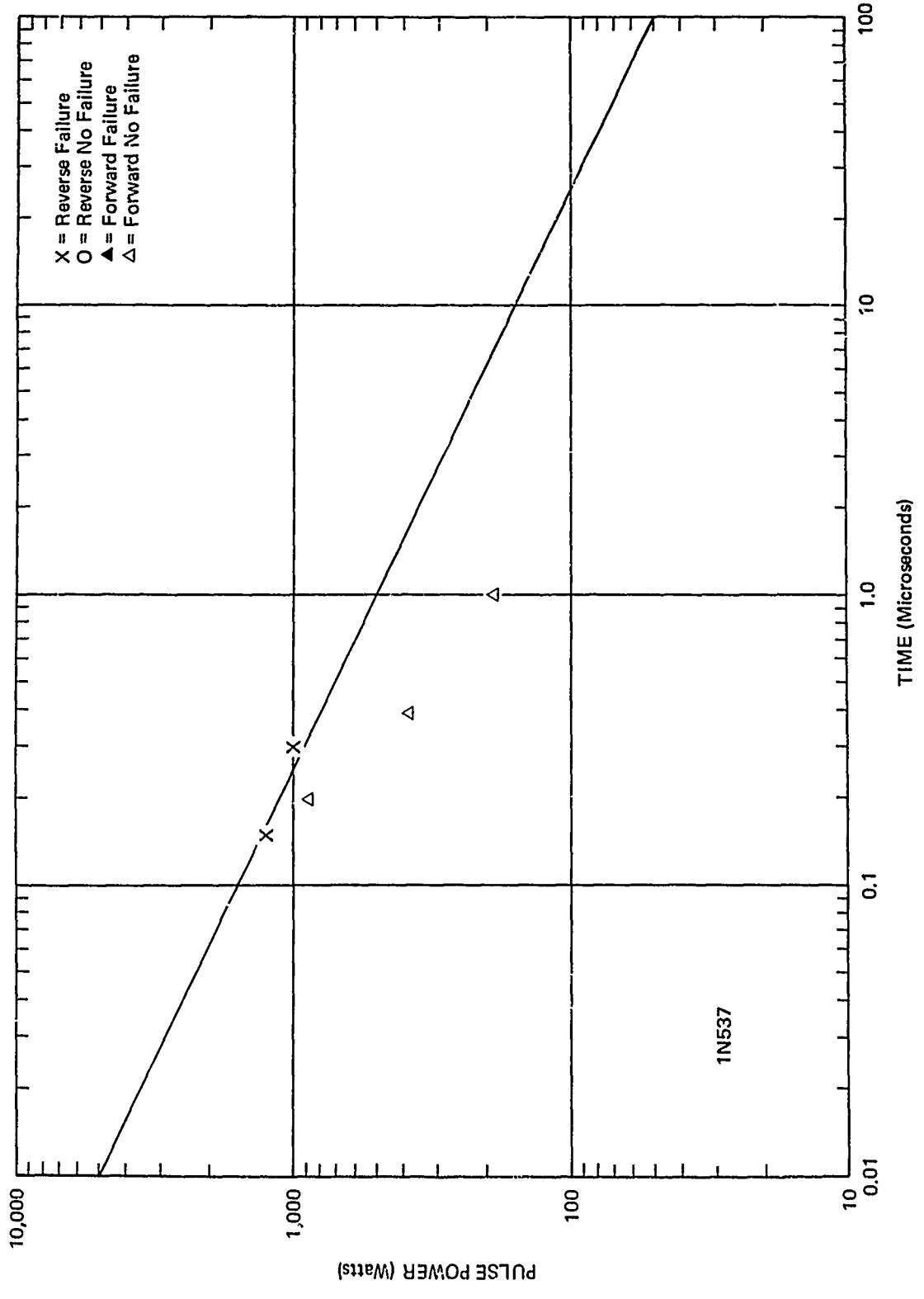
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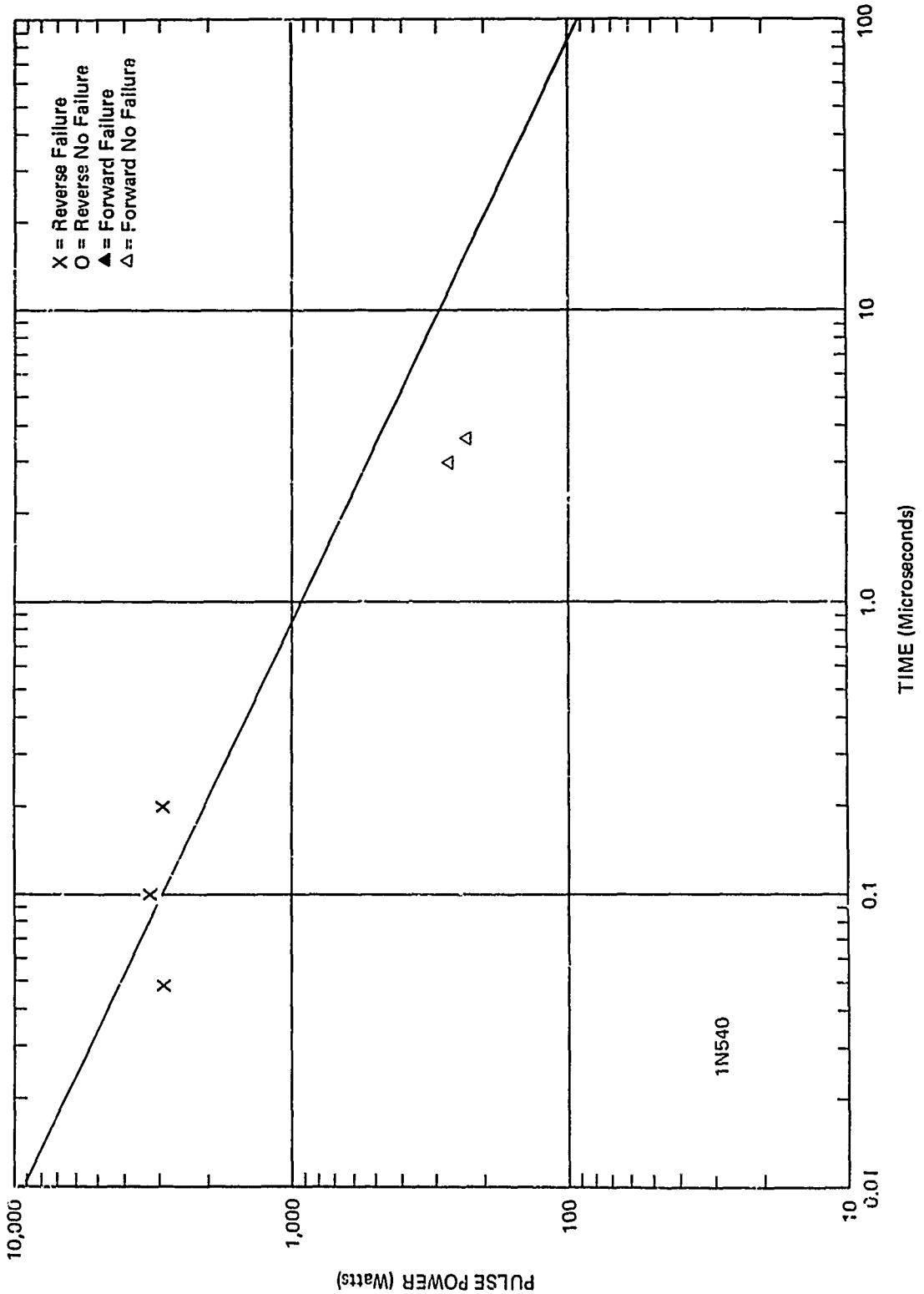
TIME (Microseconds)

3.21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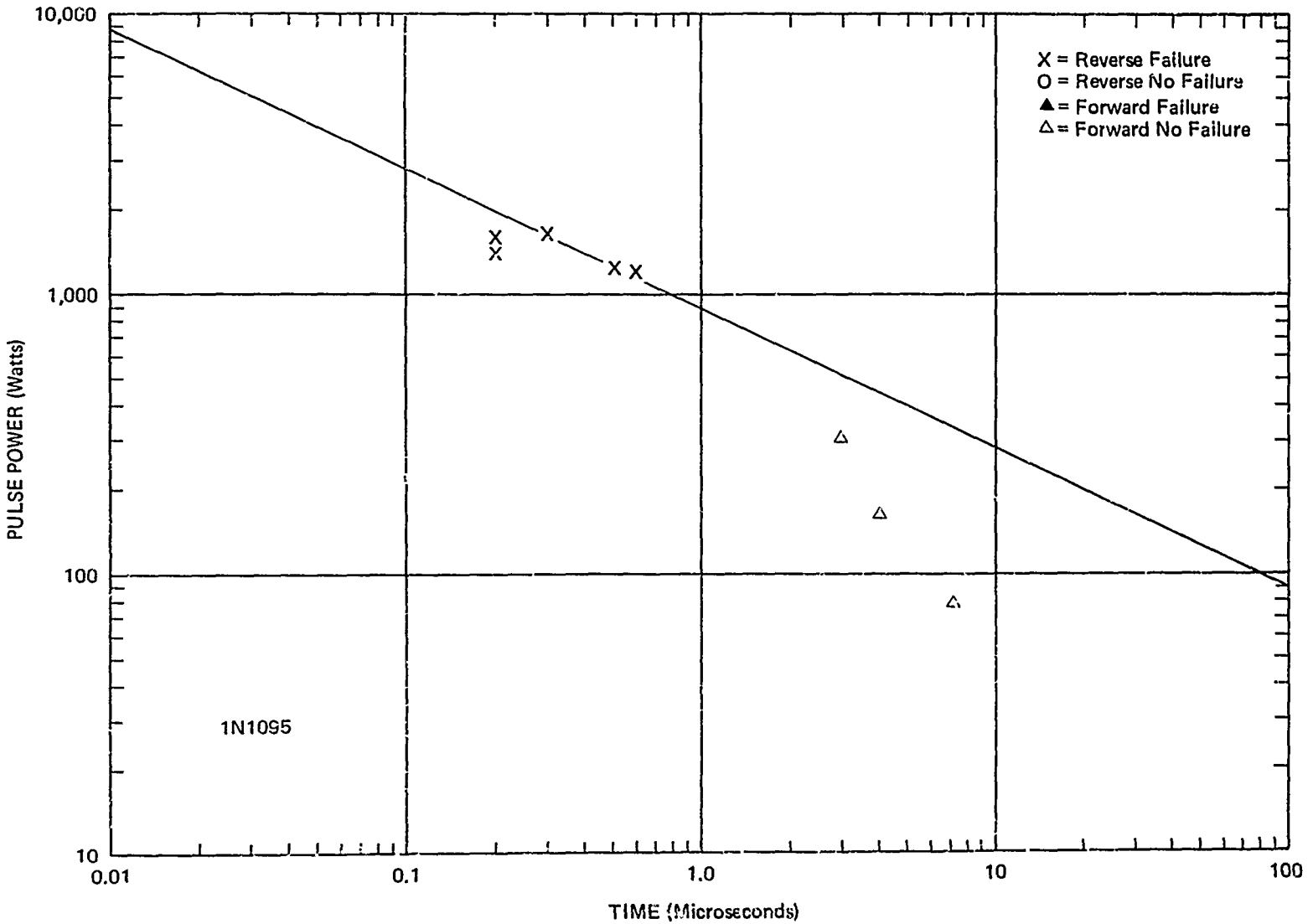
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0.01
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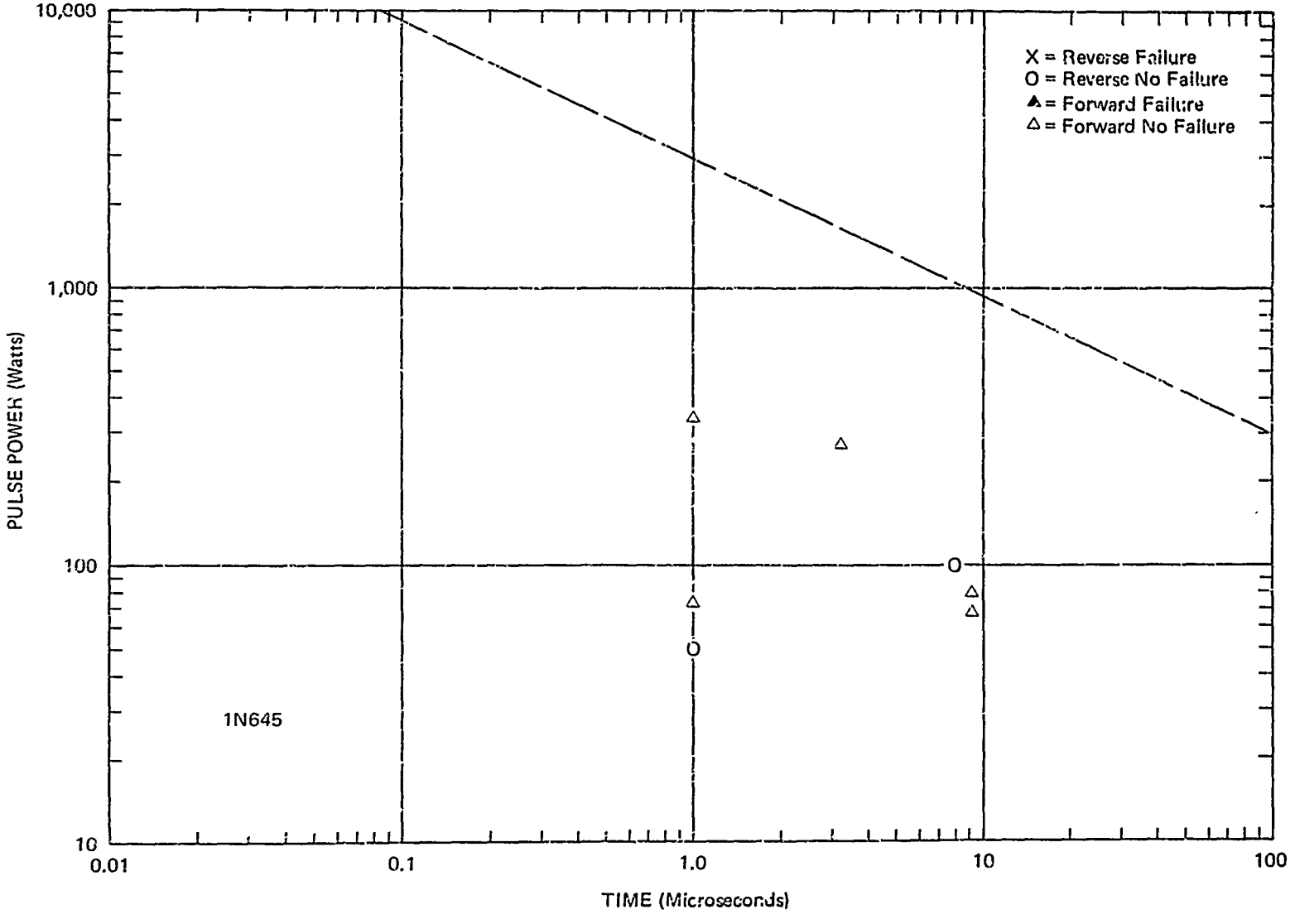
1N1095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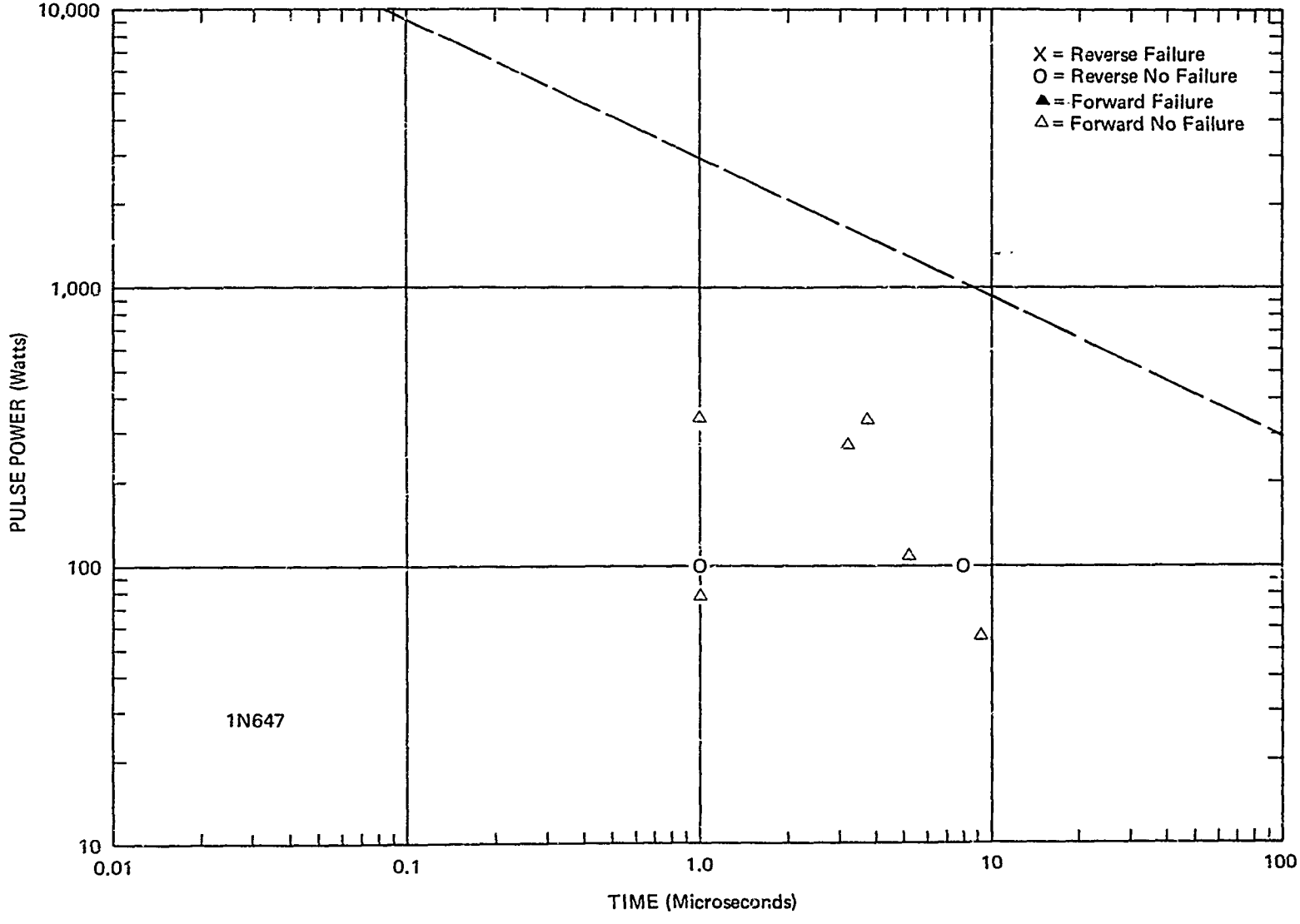
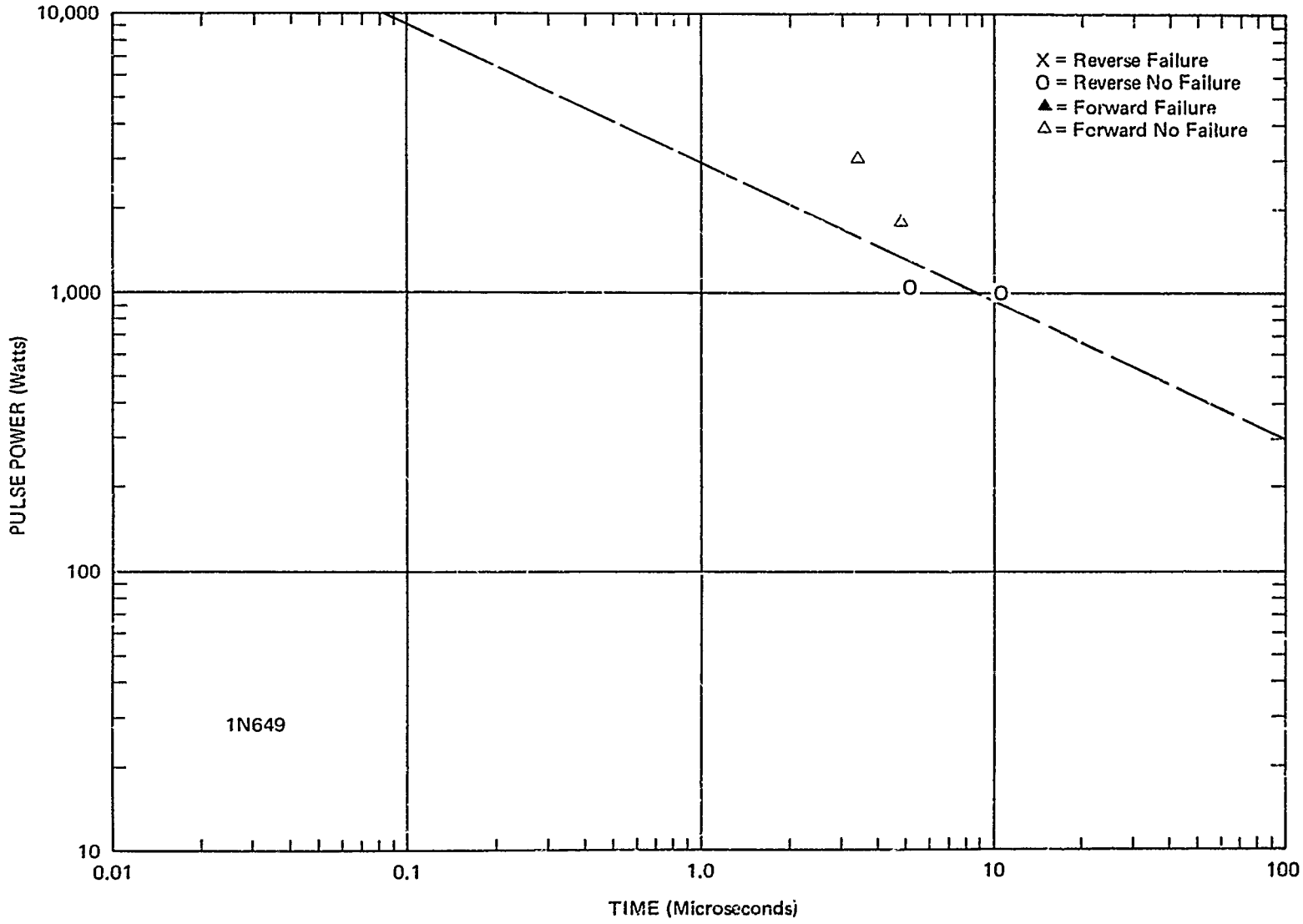
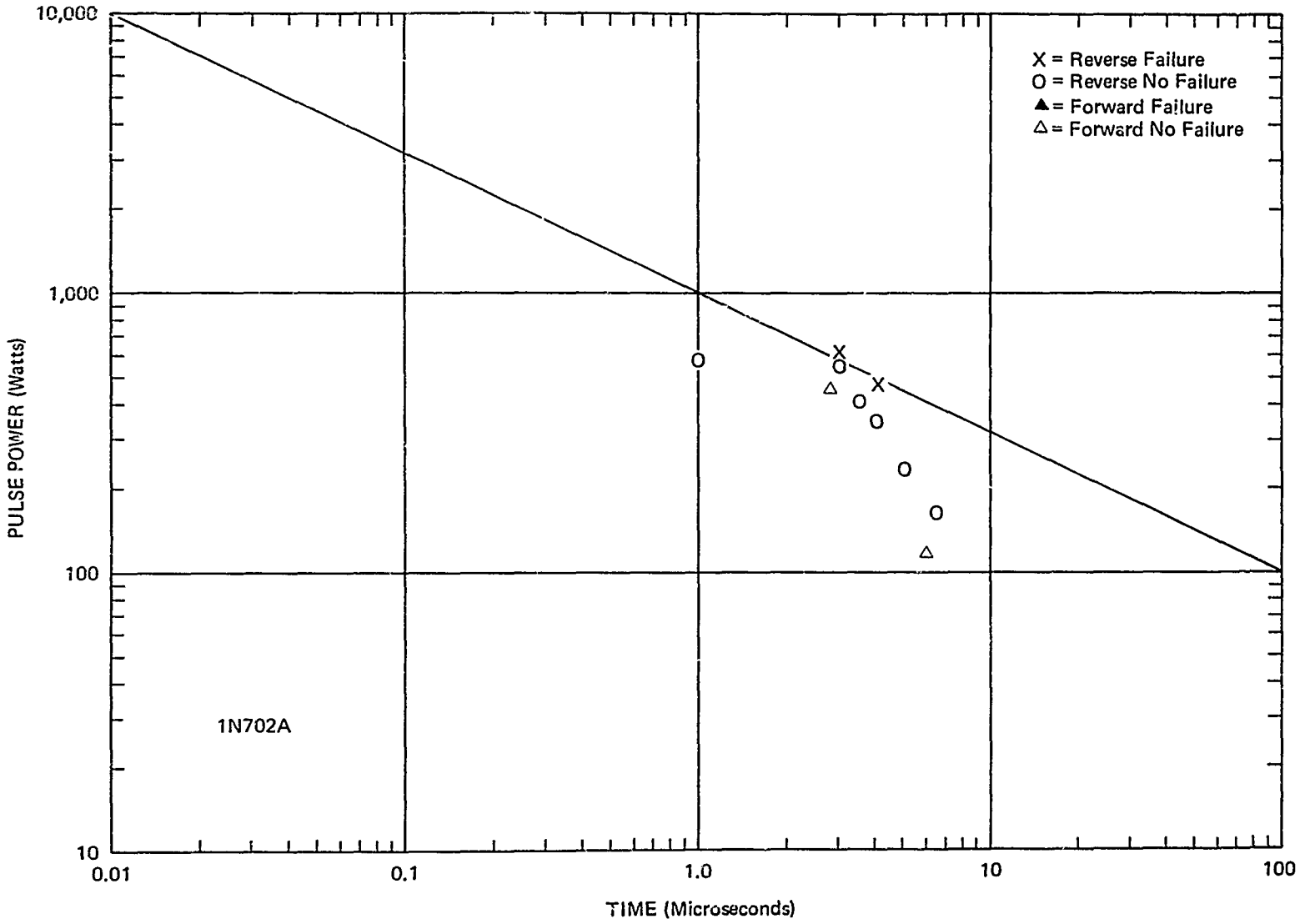
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N645

3.24


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N647

3.25


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N649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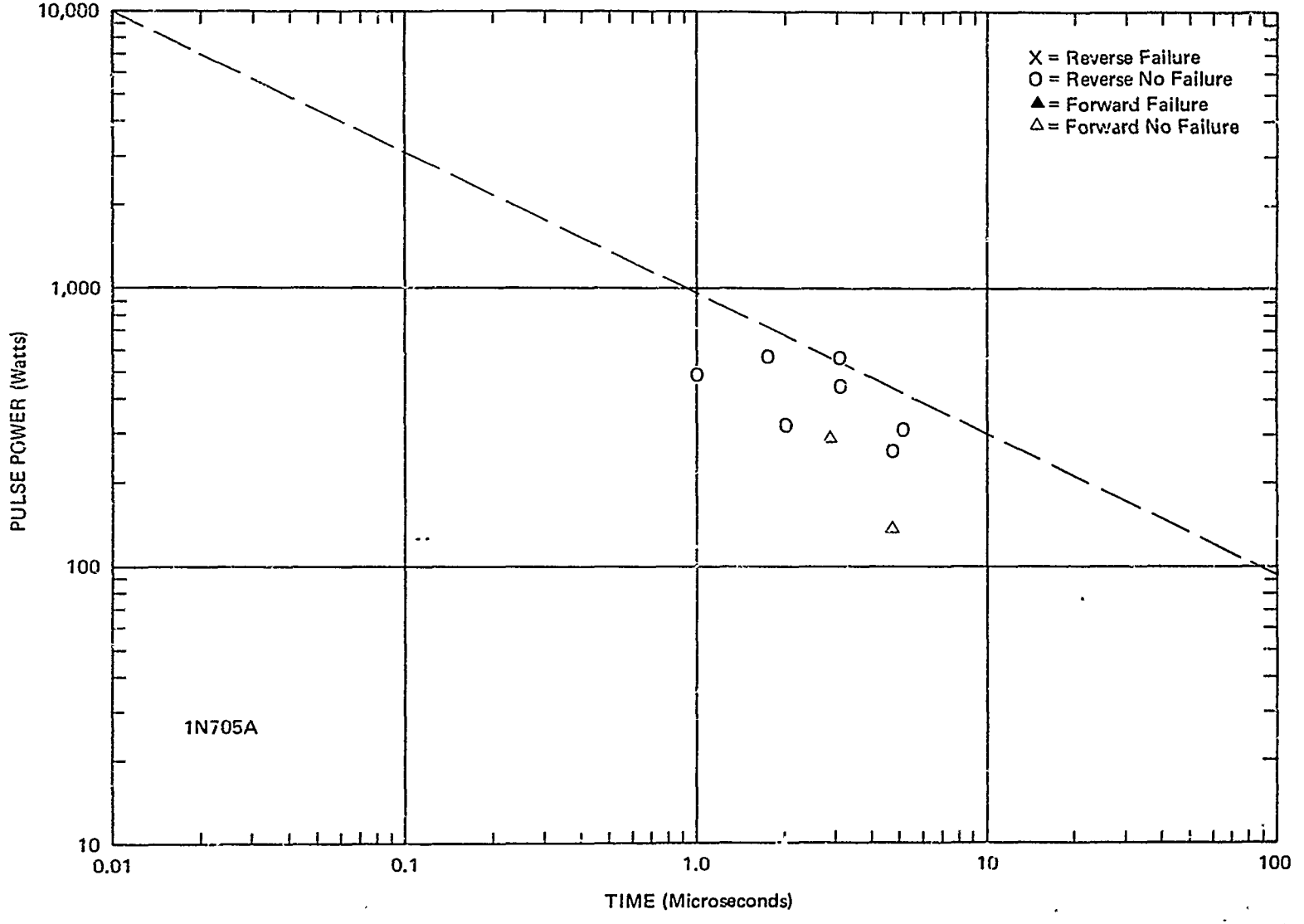
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N702A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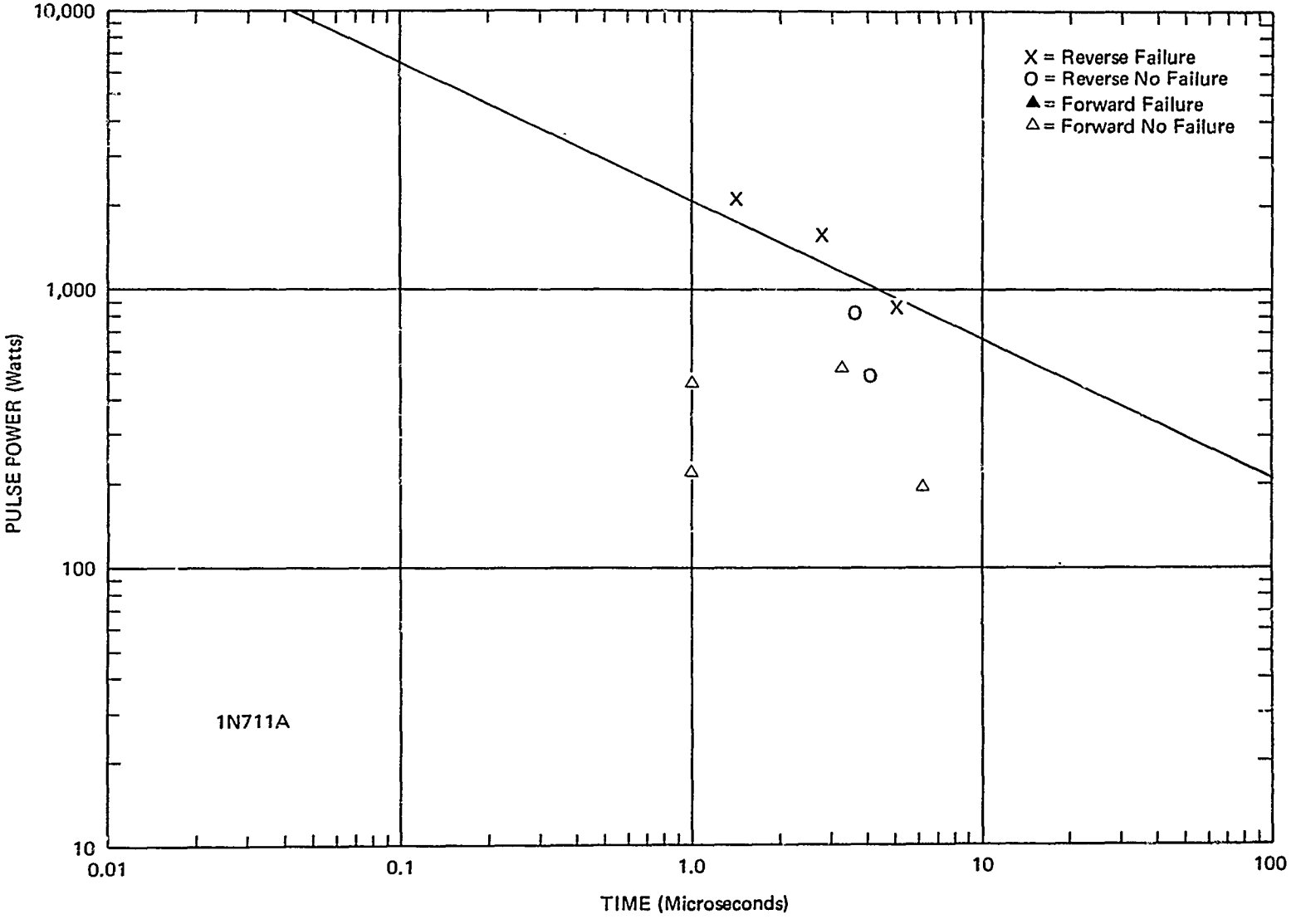
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N705A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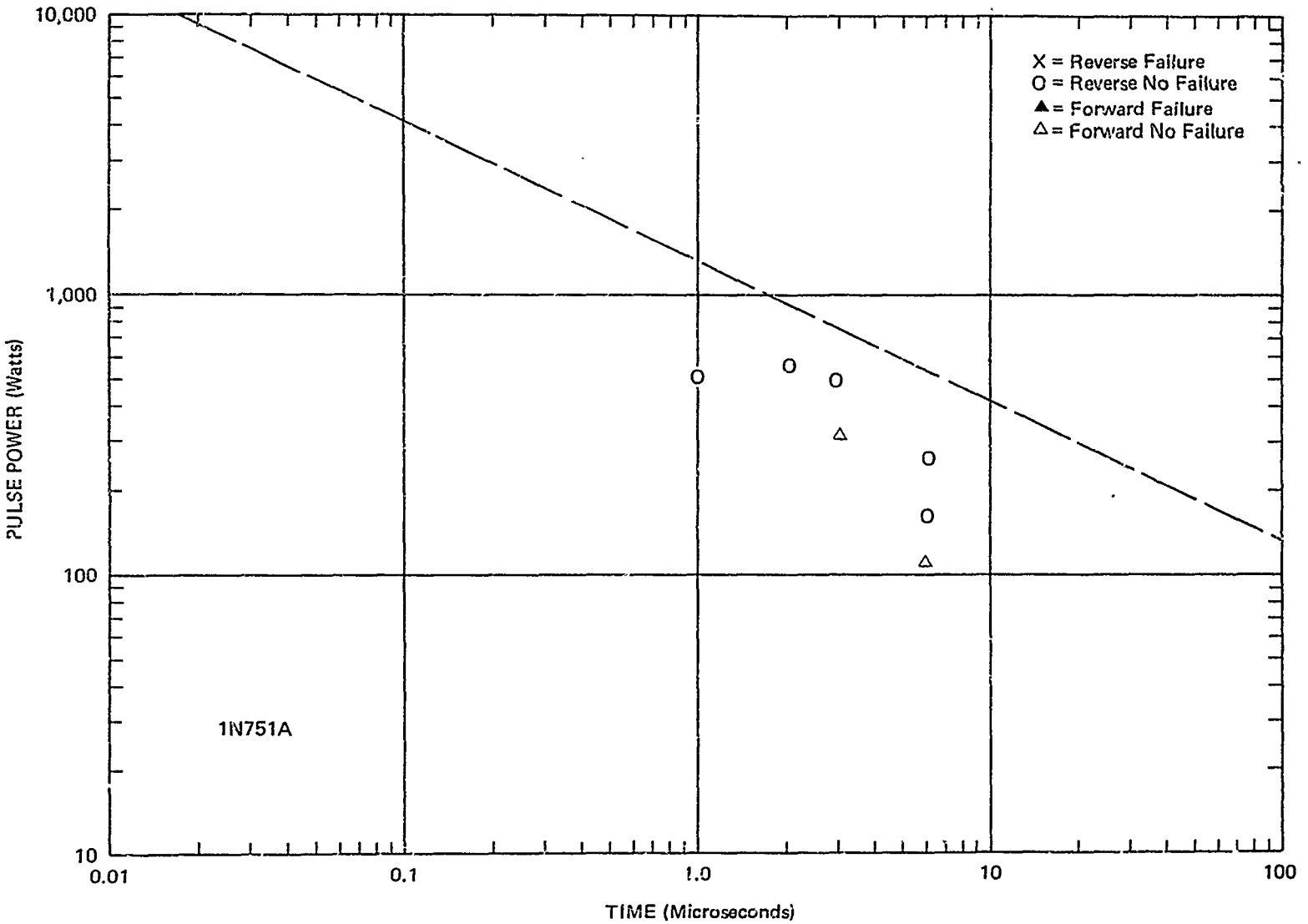
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N711A

3.29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1,000
100
10
0.01
0.1
1.0
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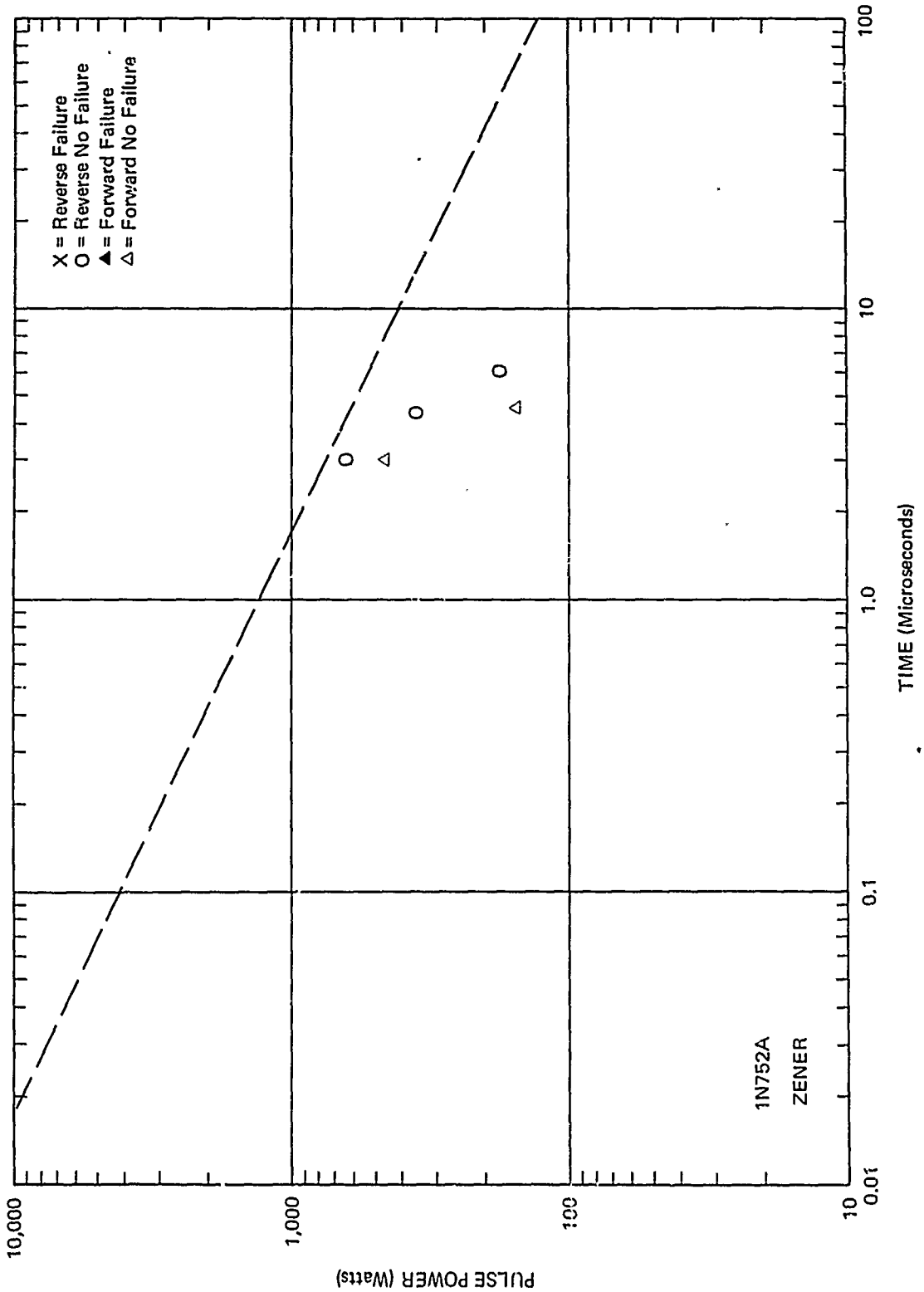
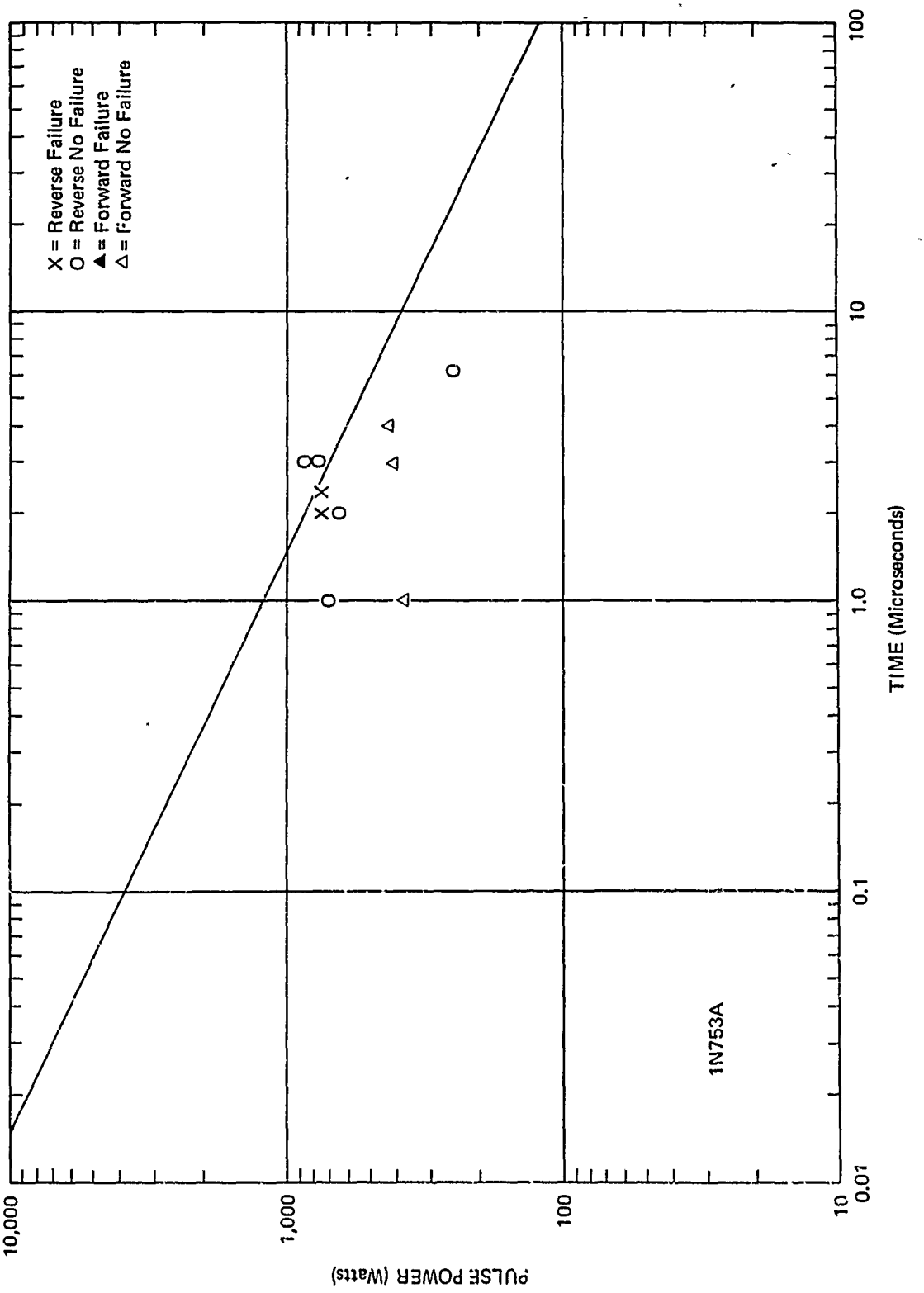
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N751A


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N752A
ZENER
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.31


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N753A
PULSE POWER (Watts)
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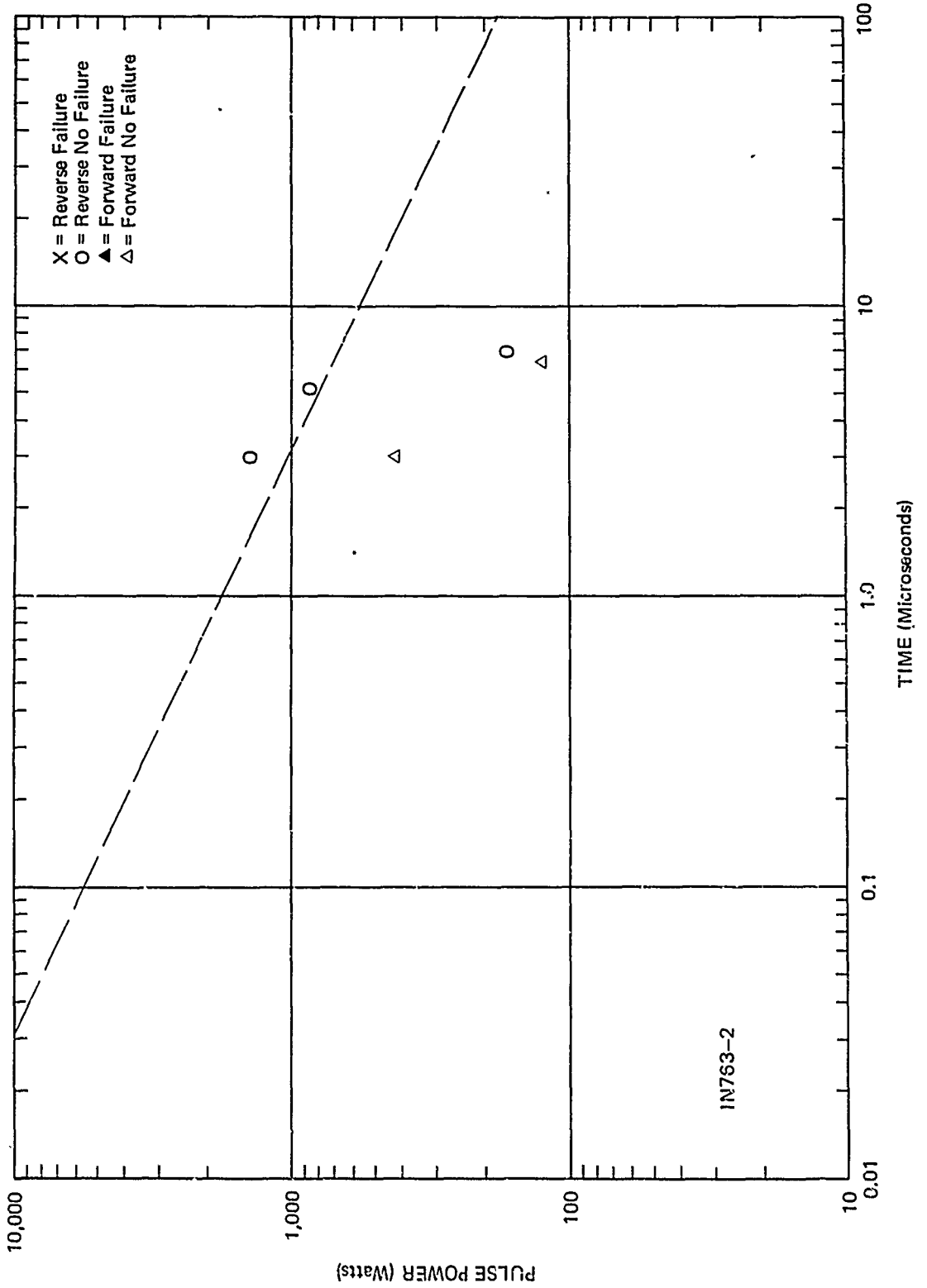
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.32


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N763-2
PULSE POWER (Watts)
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1,000
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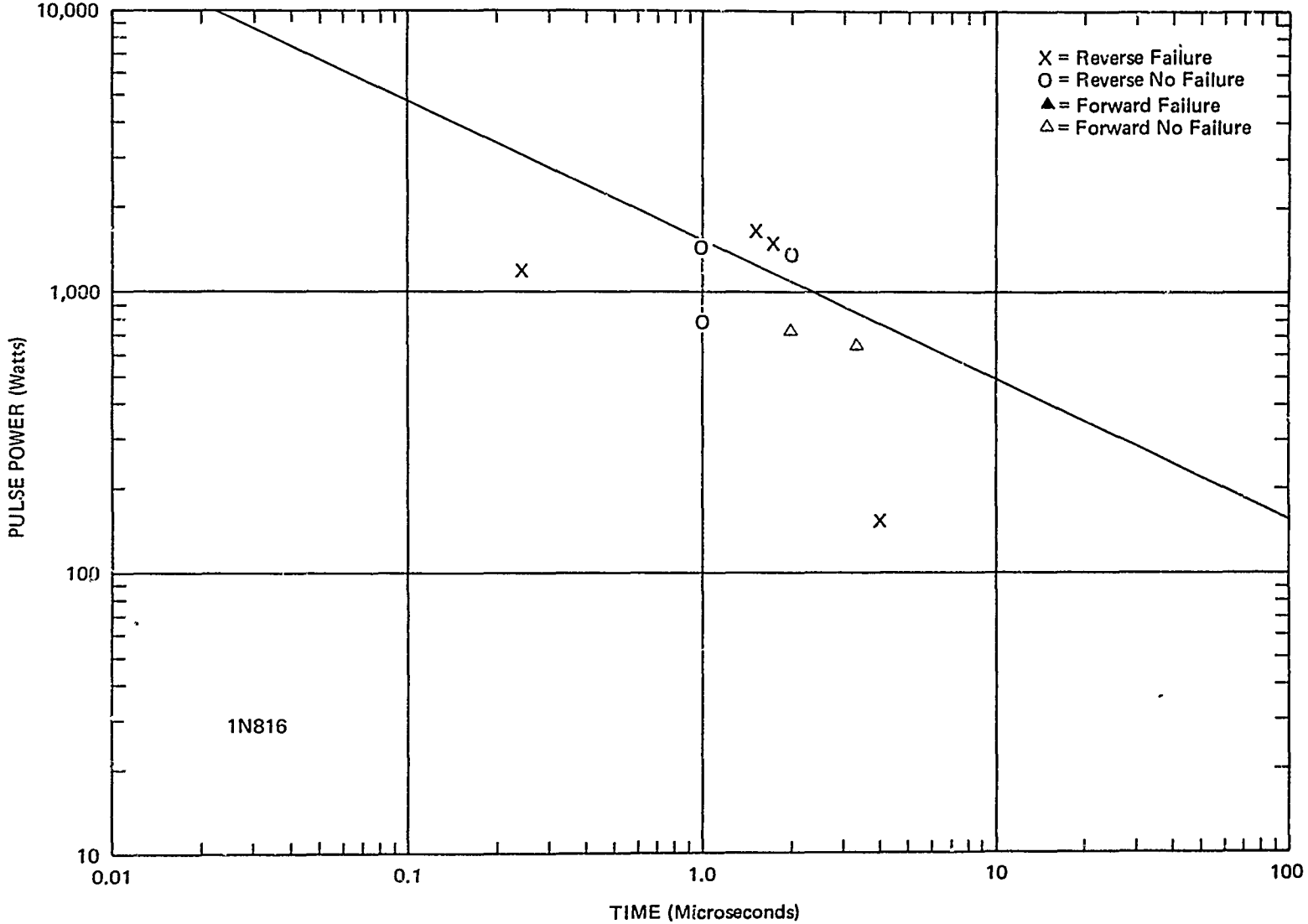
0.1
1.0
10
100
TIME (Microseconds)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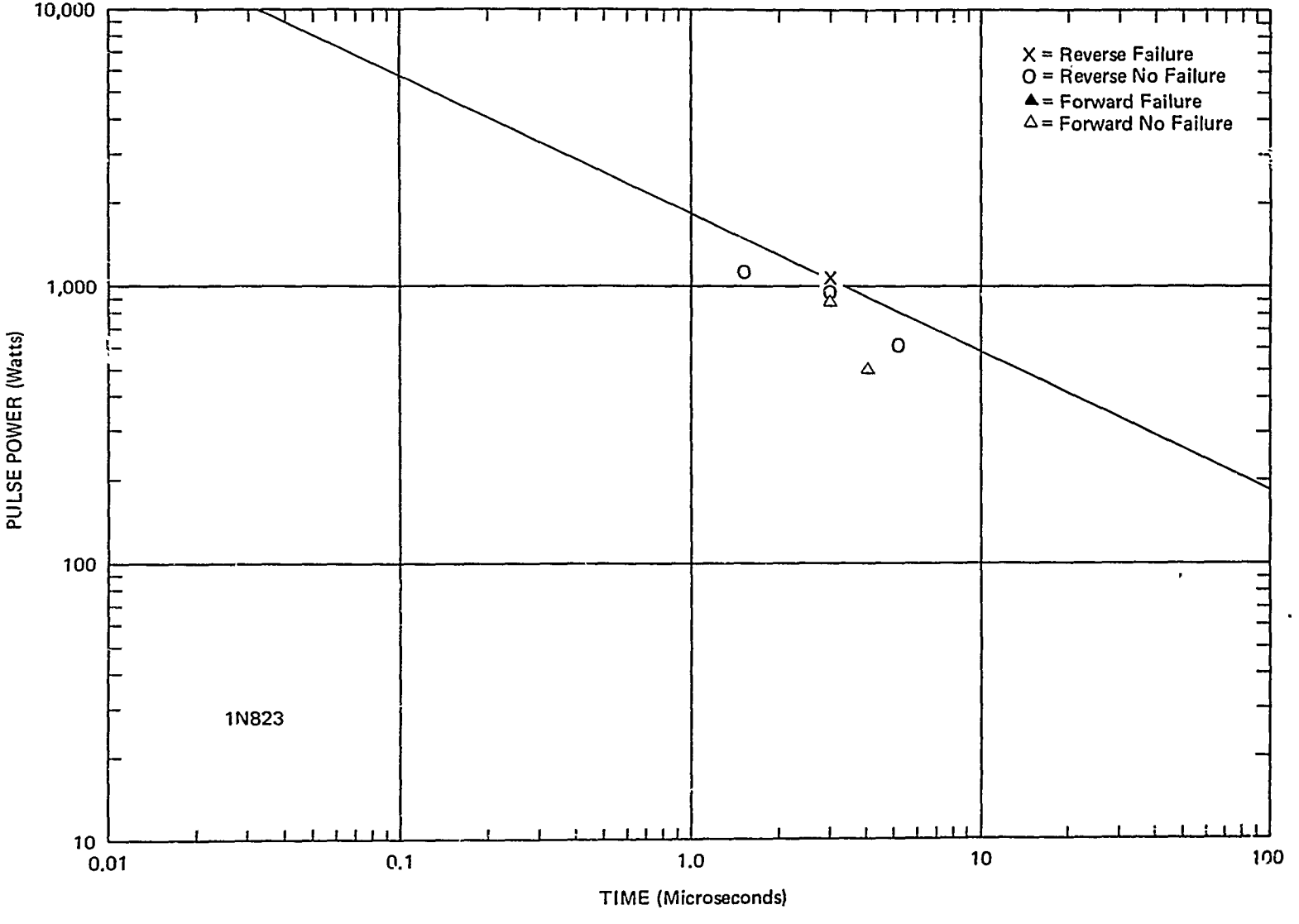
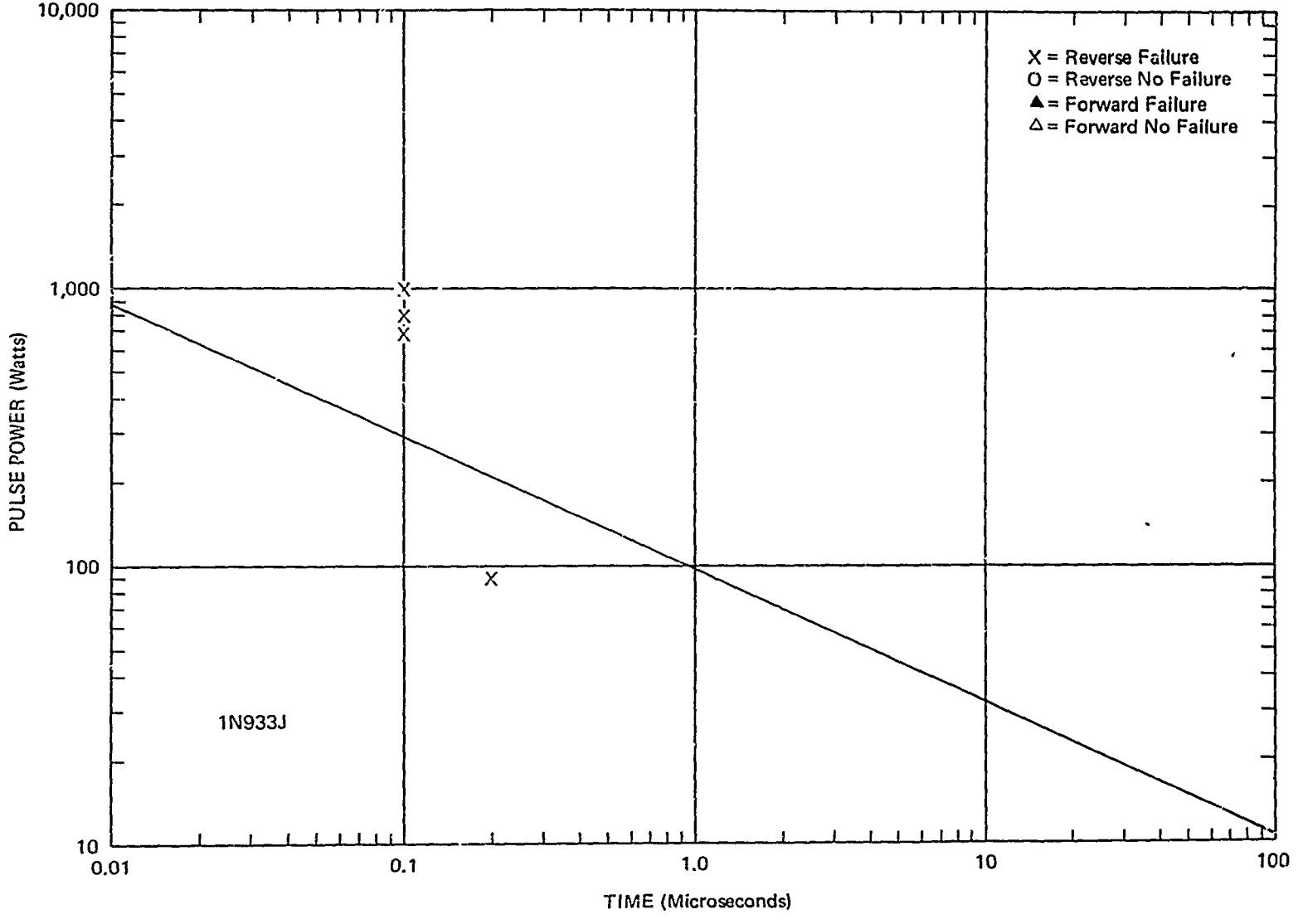
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N816

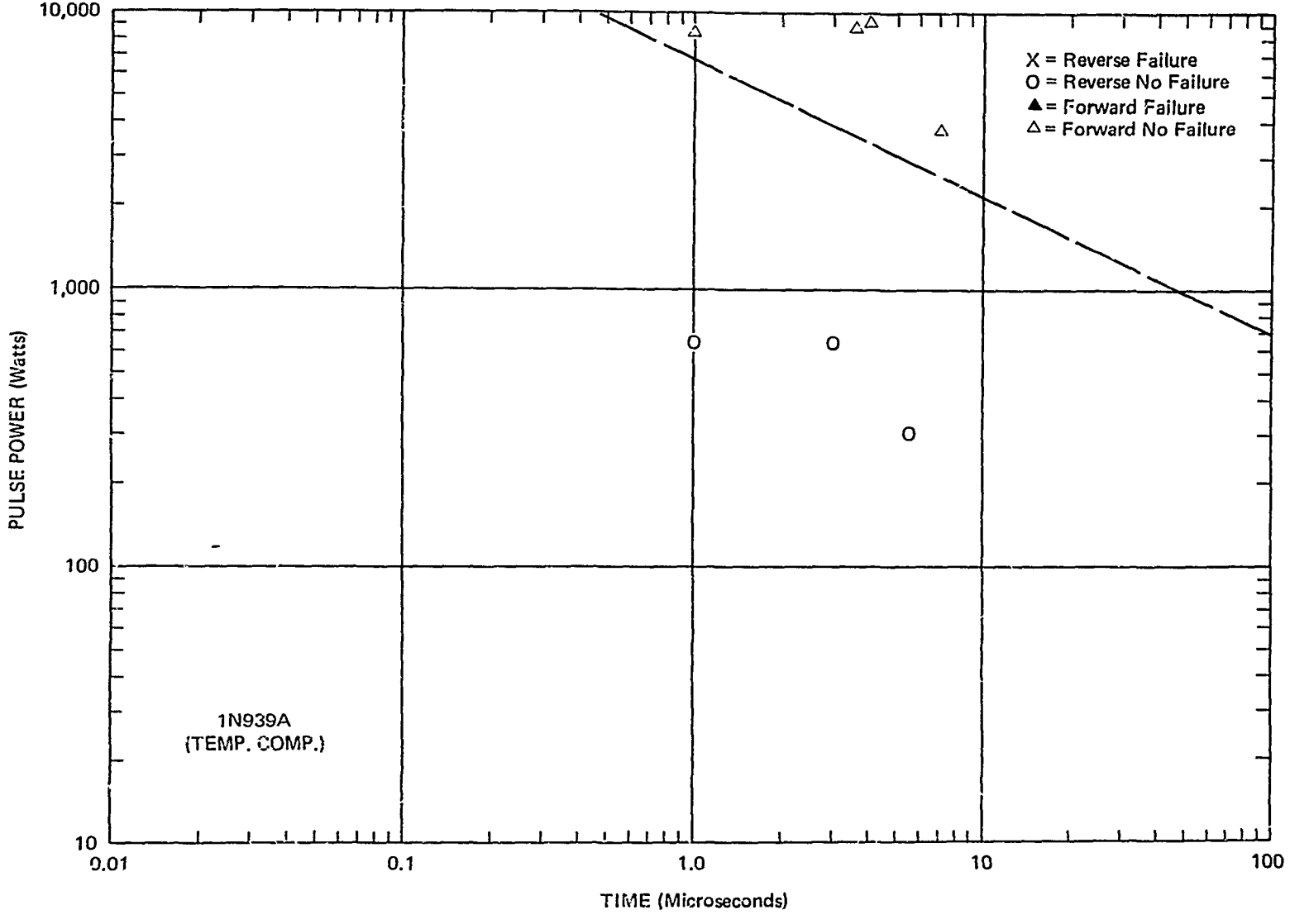
3.34

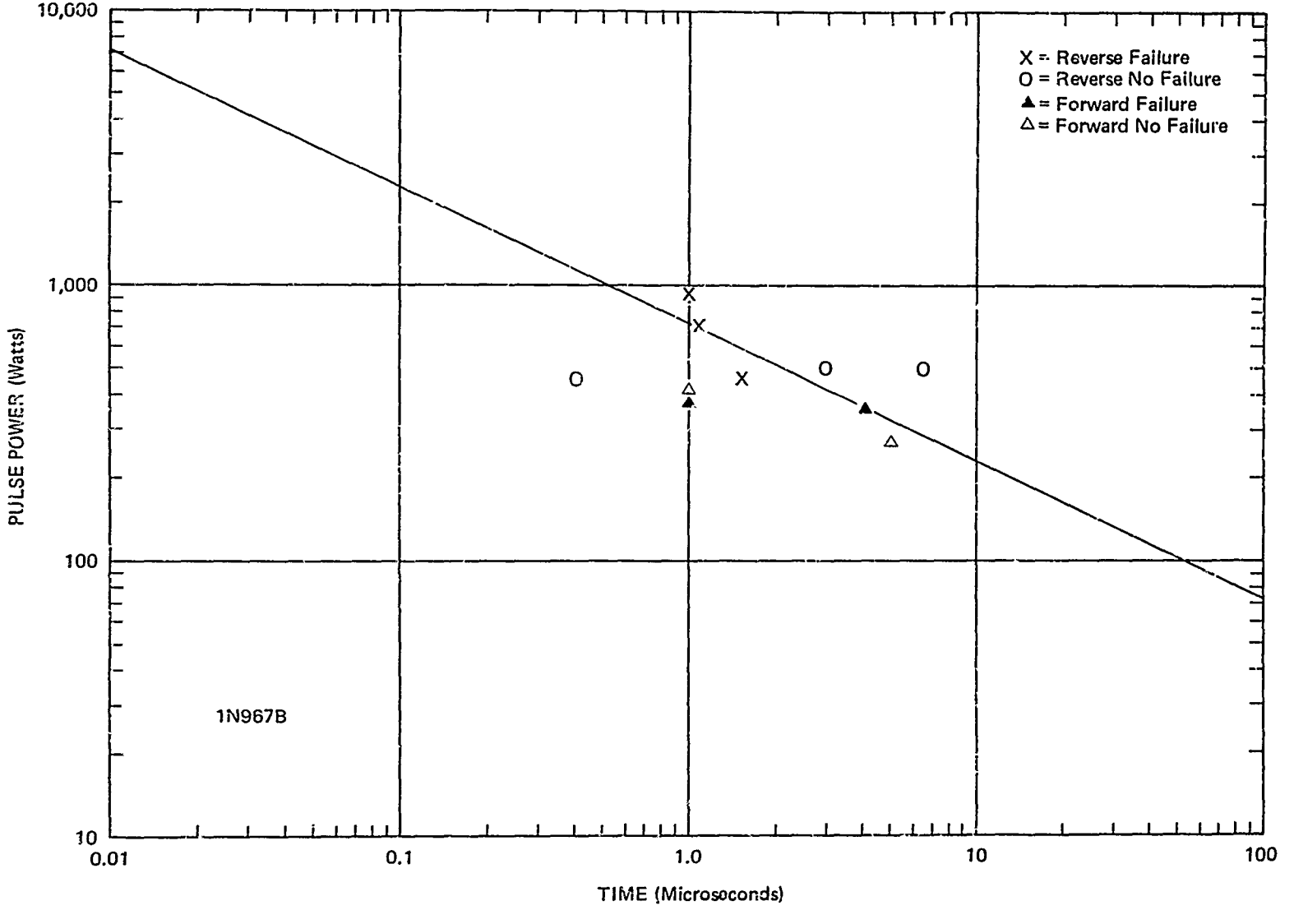

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N823

3.35

K′ = 1.8

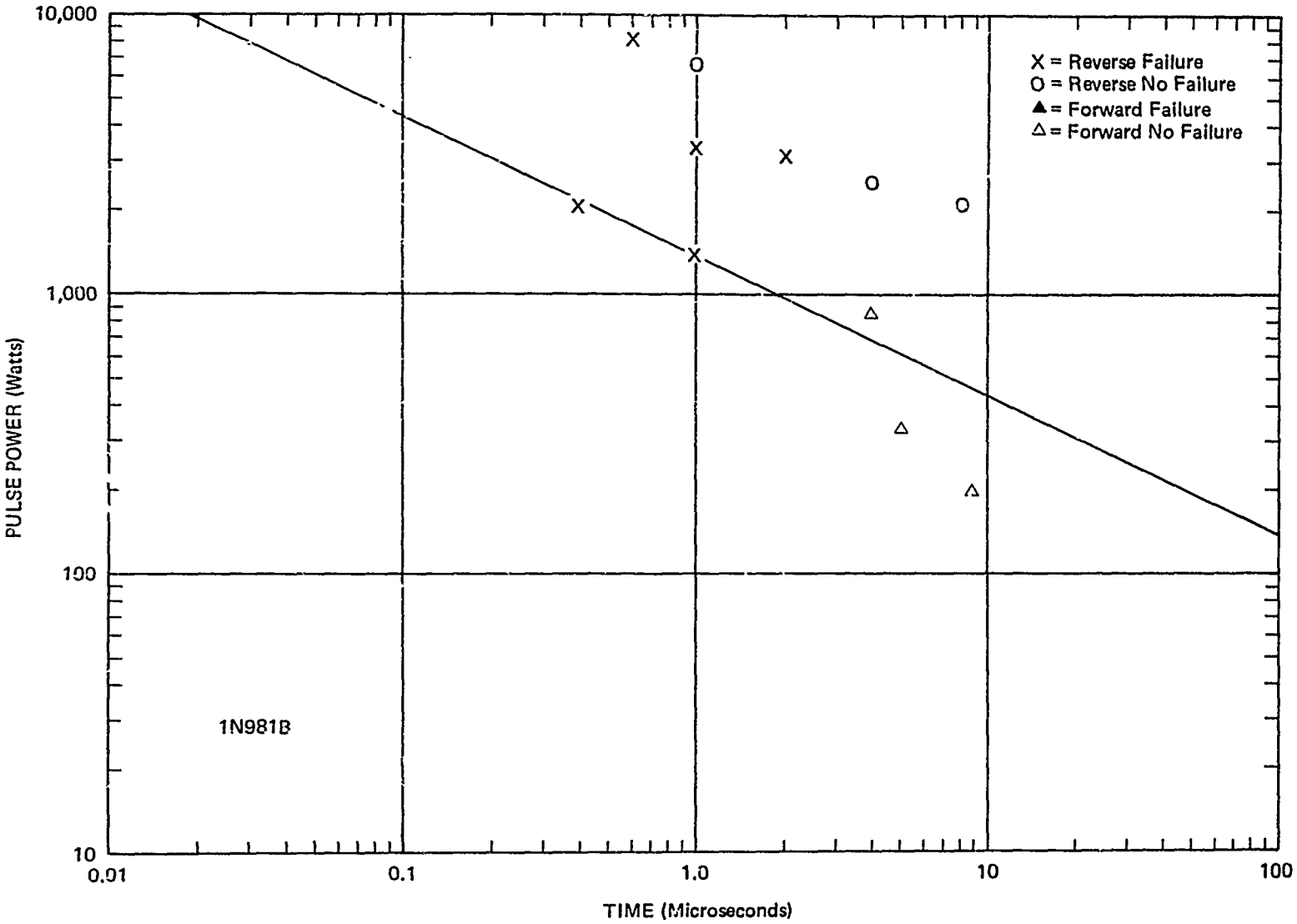

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N933J


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N939A
(TEMP. COMP.)

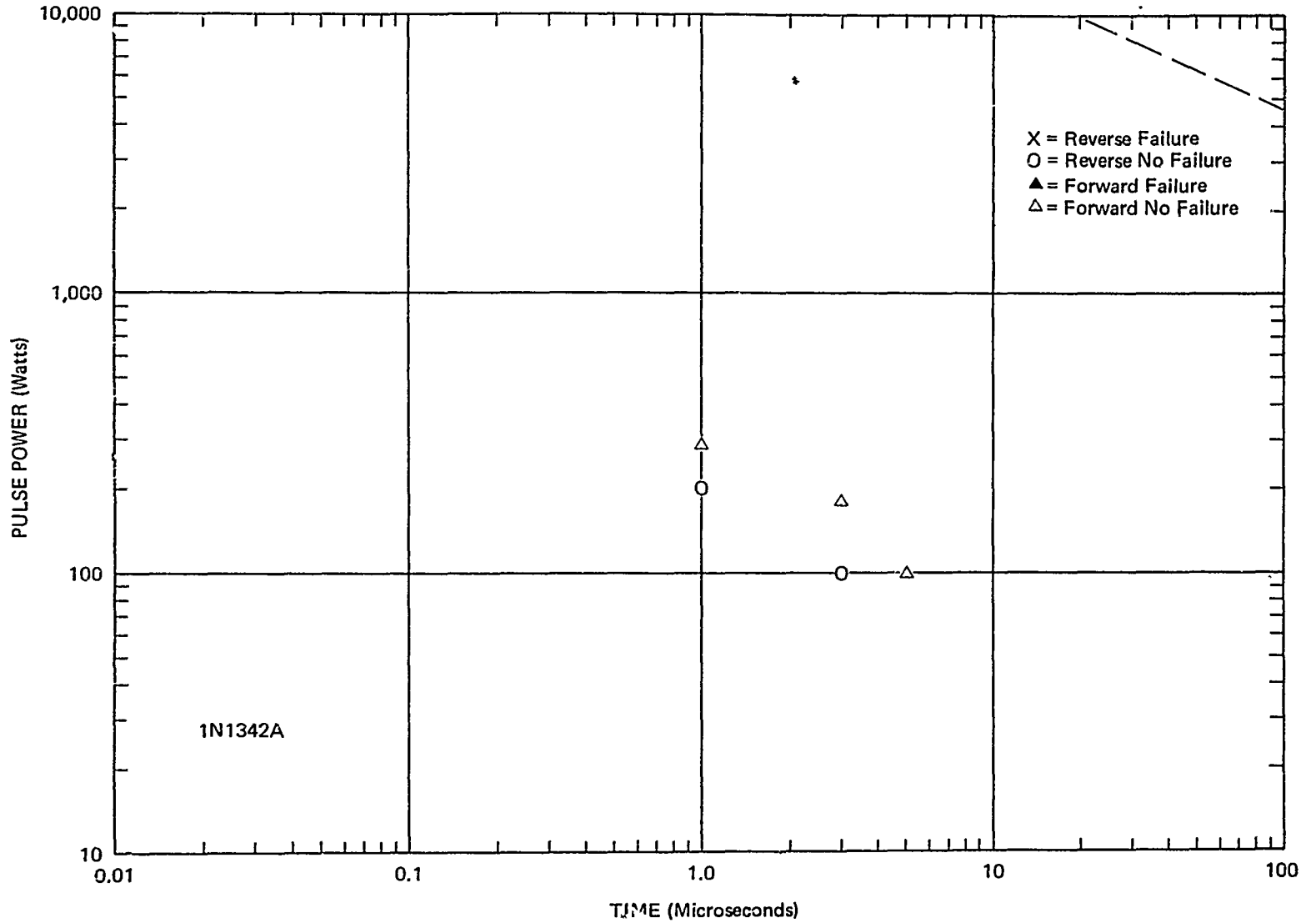

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N967B

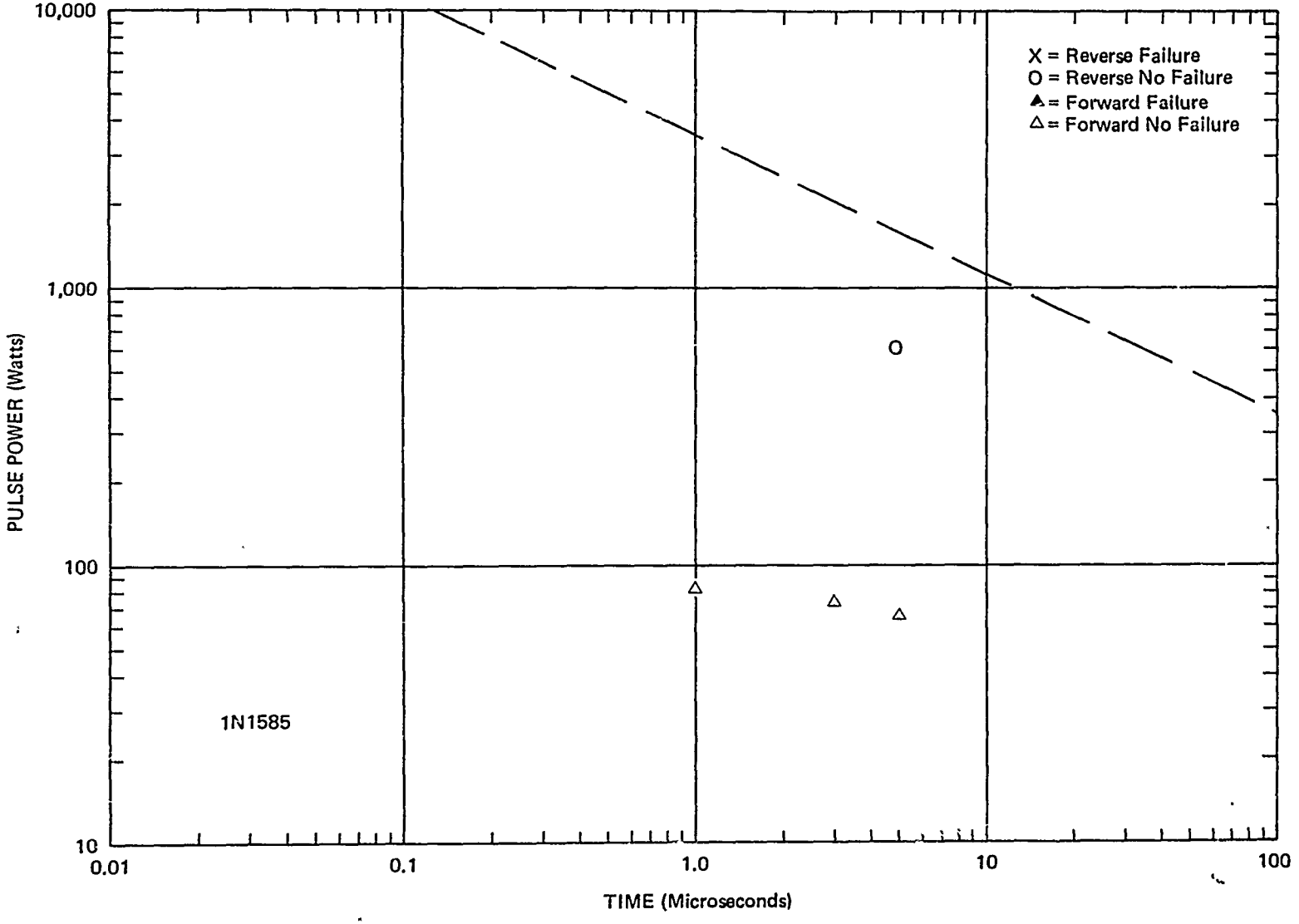
3.38

K' = .73


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N981B

3.39

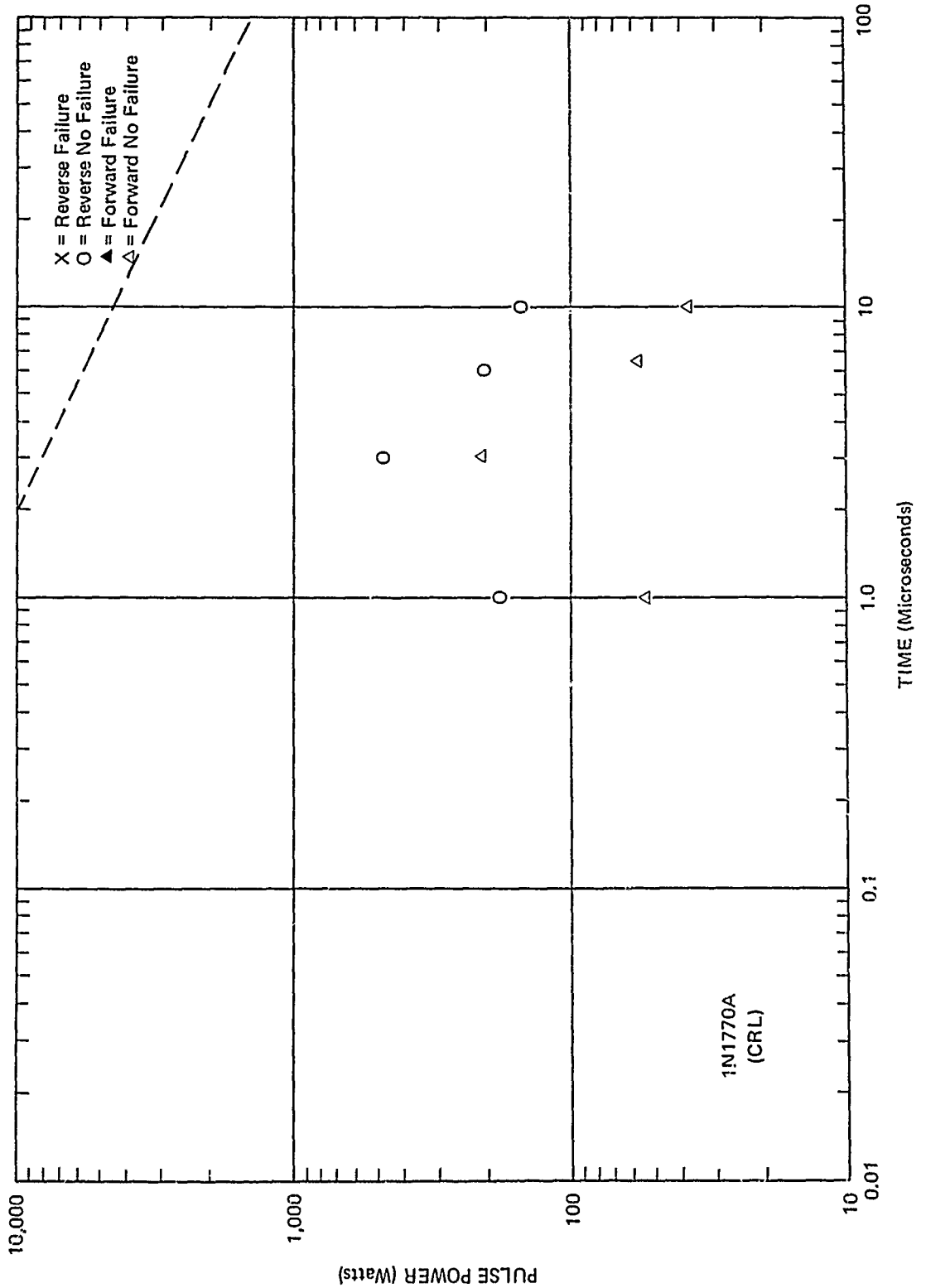

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N1342A


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲= Forward Failure
△= Forward No Failure
O
△
△
△
1N1585

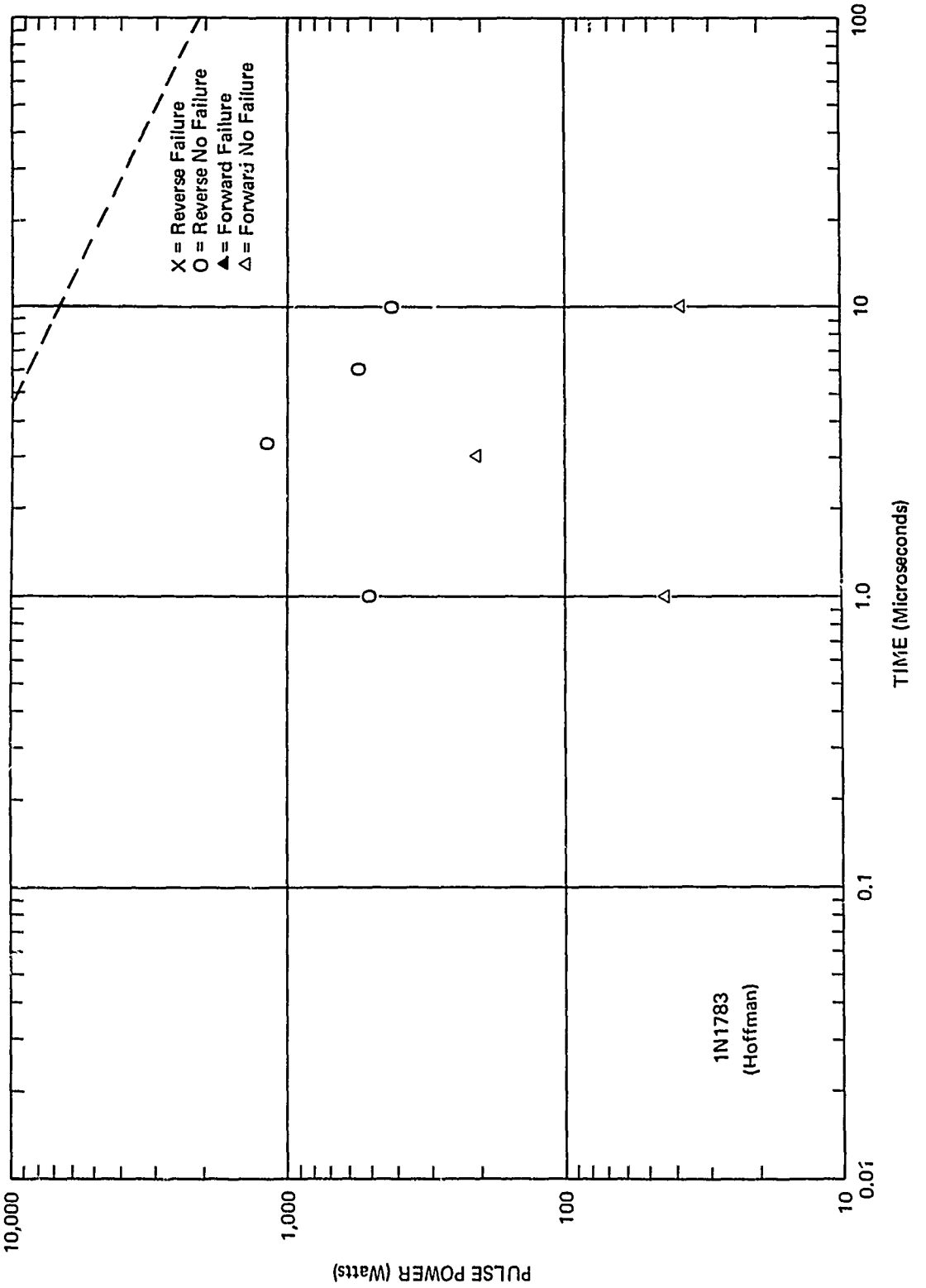
3.41

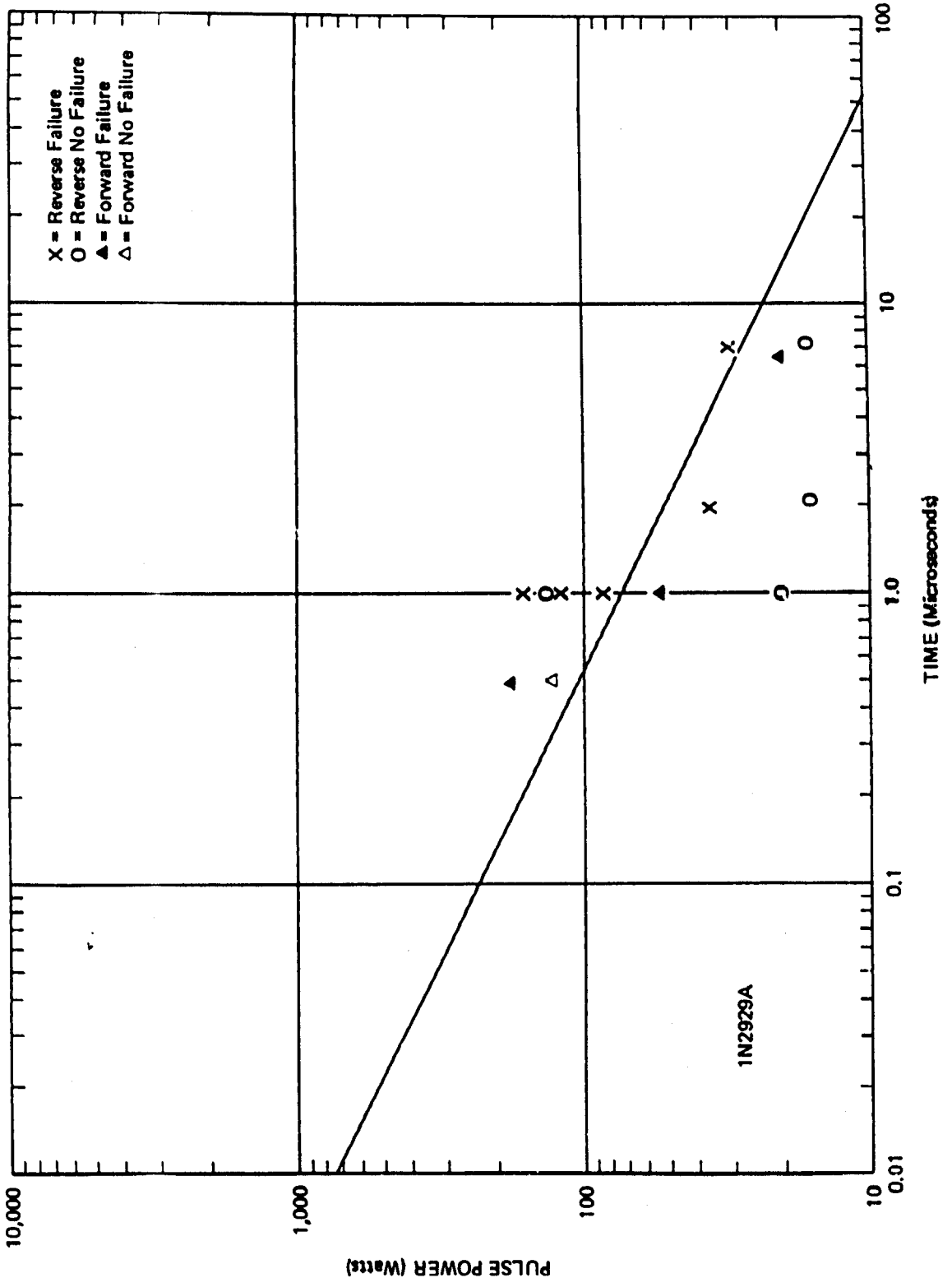
95

K' = 3.5

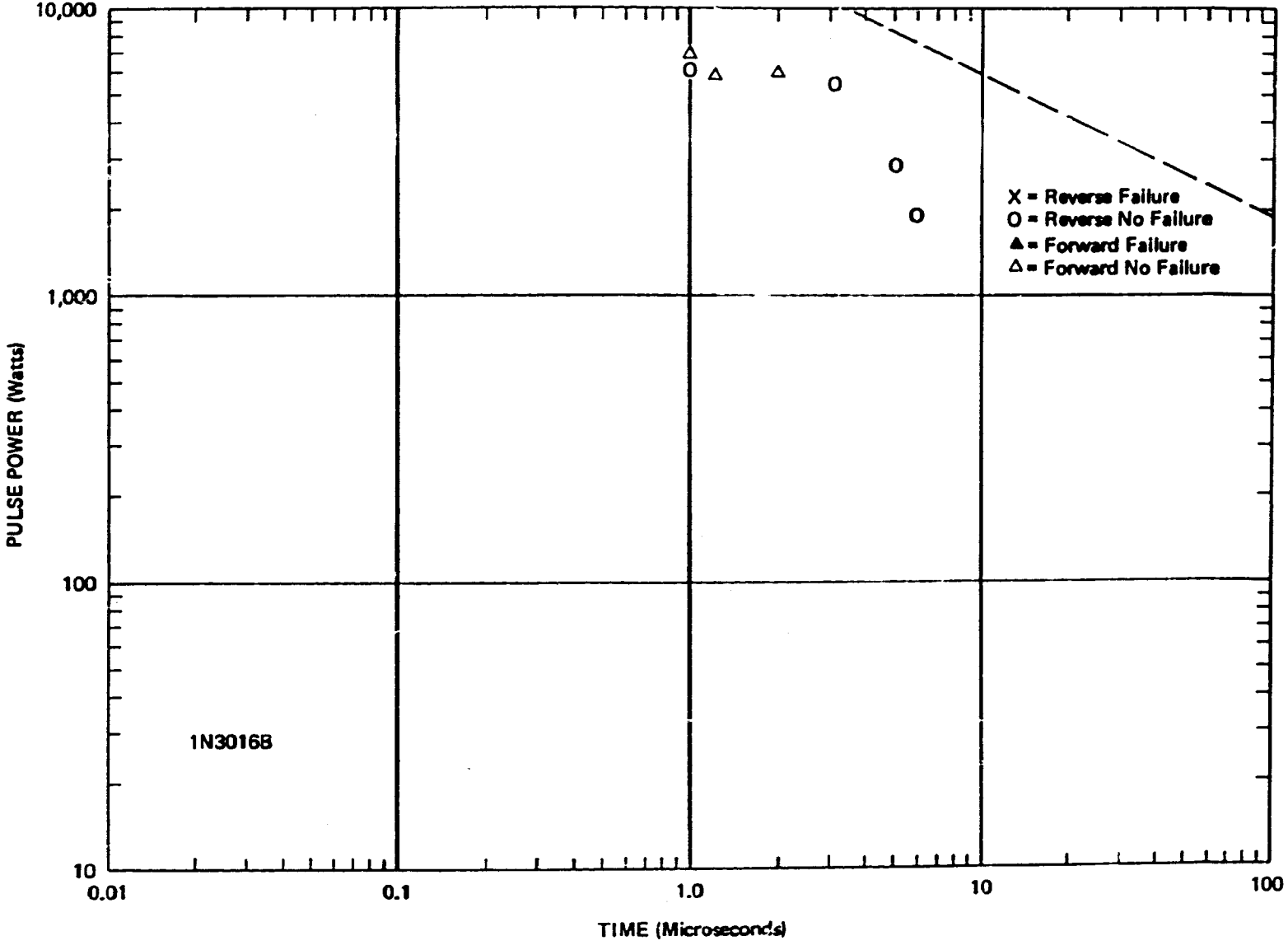

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N1770A
(CRL)
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.42

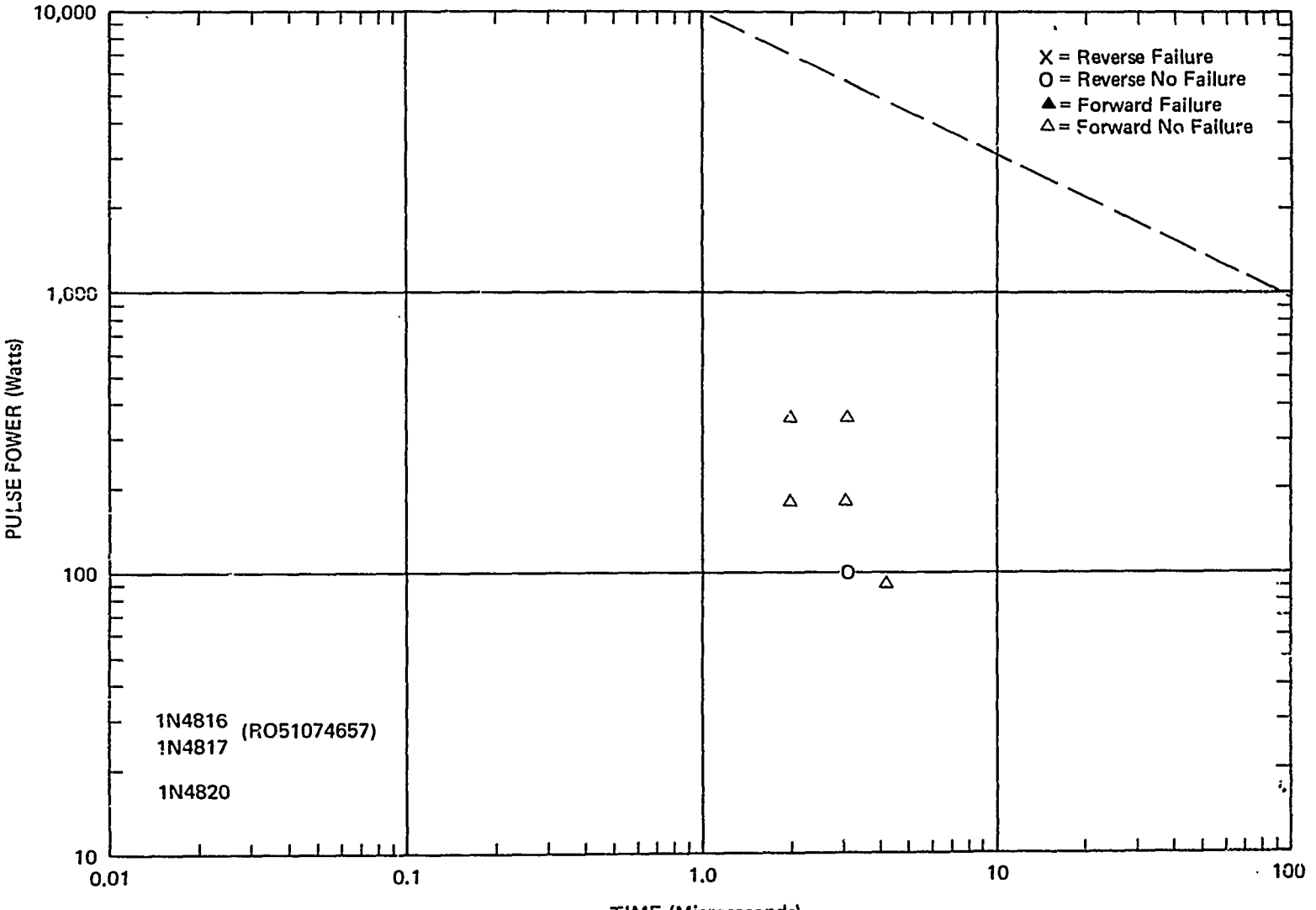

X = Reverse Failure
O = Reverse No Failure
▲= Forward Failure
△= Forward No Failure
1N1783
(Hoffman)
PULSE POWER (Watts)
10,000
1,000
100
10
TIME (Microseconds)
0.01
0.1
1.0
10
100

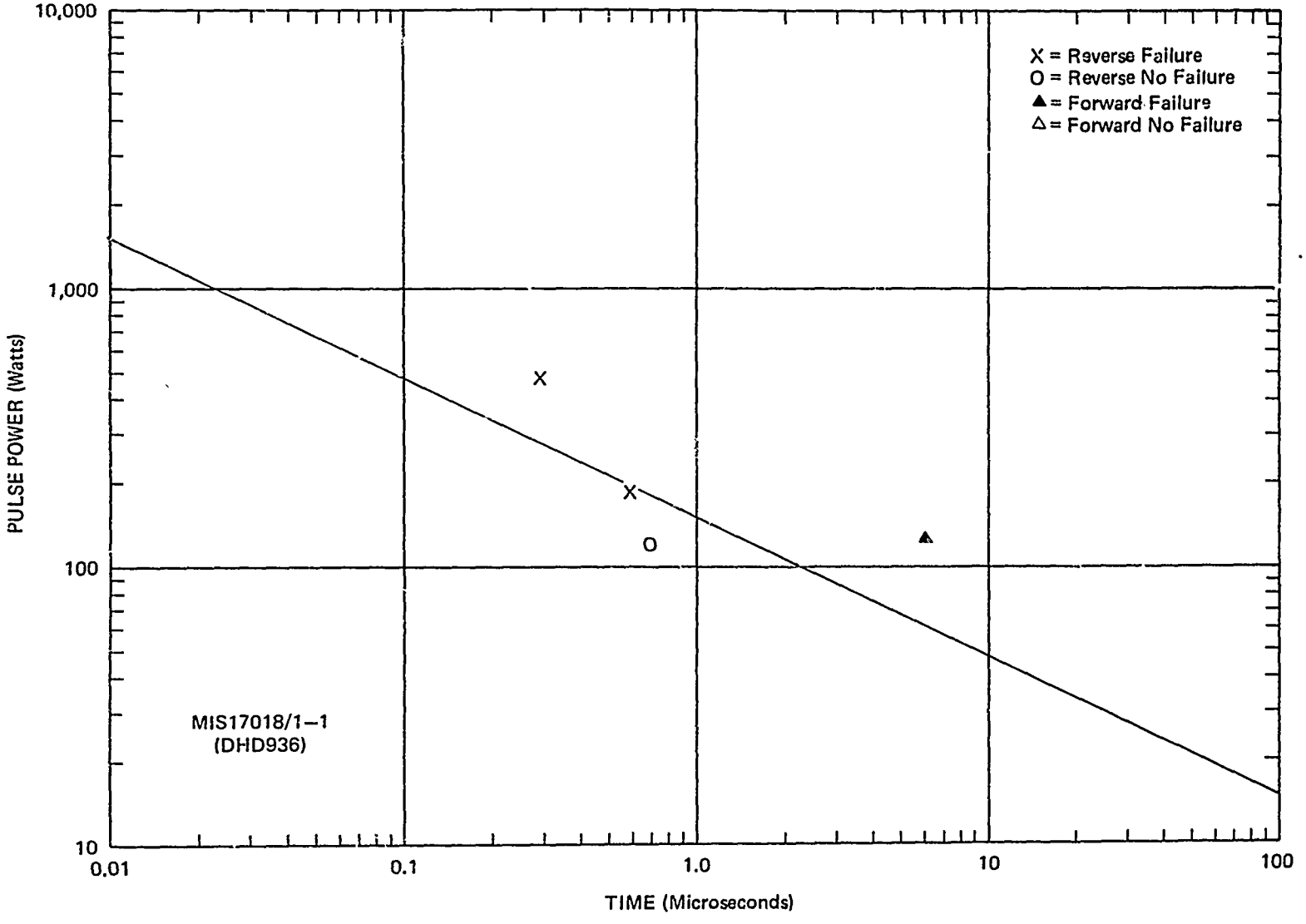

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N2929A
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.44

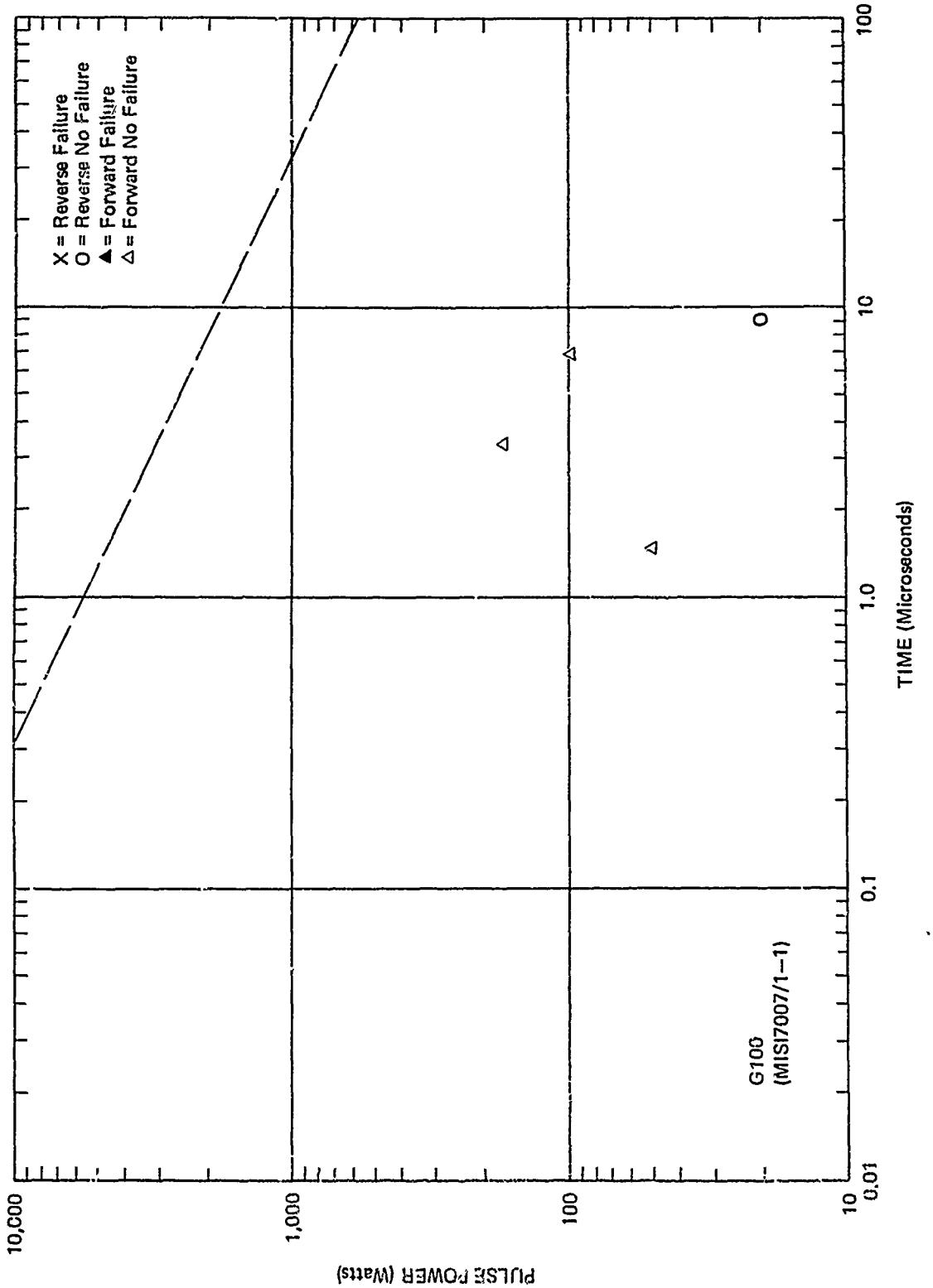

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N3016B

3.45


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
1N4816
1N4817
(RO51074657)
1N4820


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17018/1–1
(DHD936)

3.47


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
G100
(MIS17007/1-1)
PULSE POWER (Watts)
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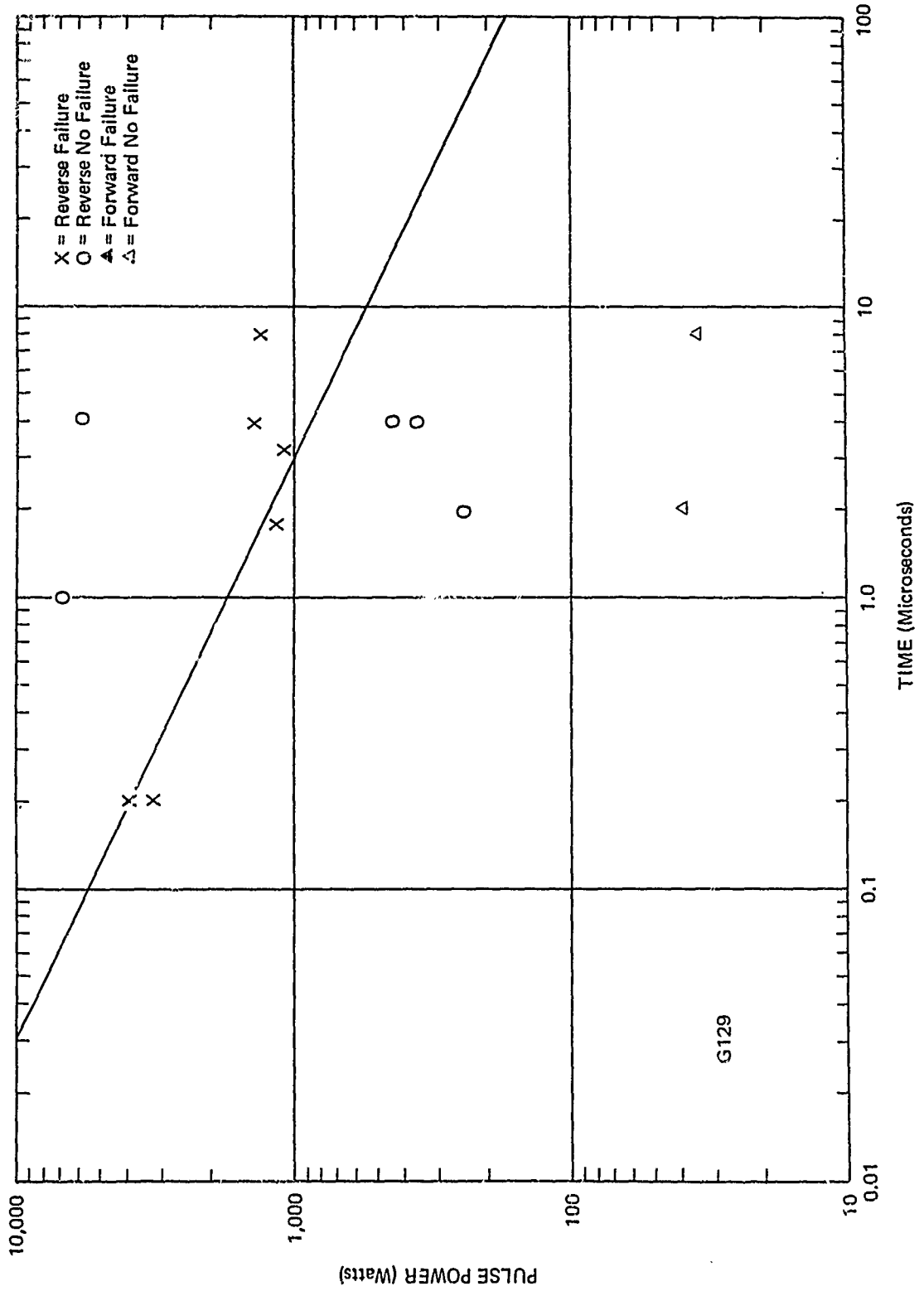
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.48


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
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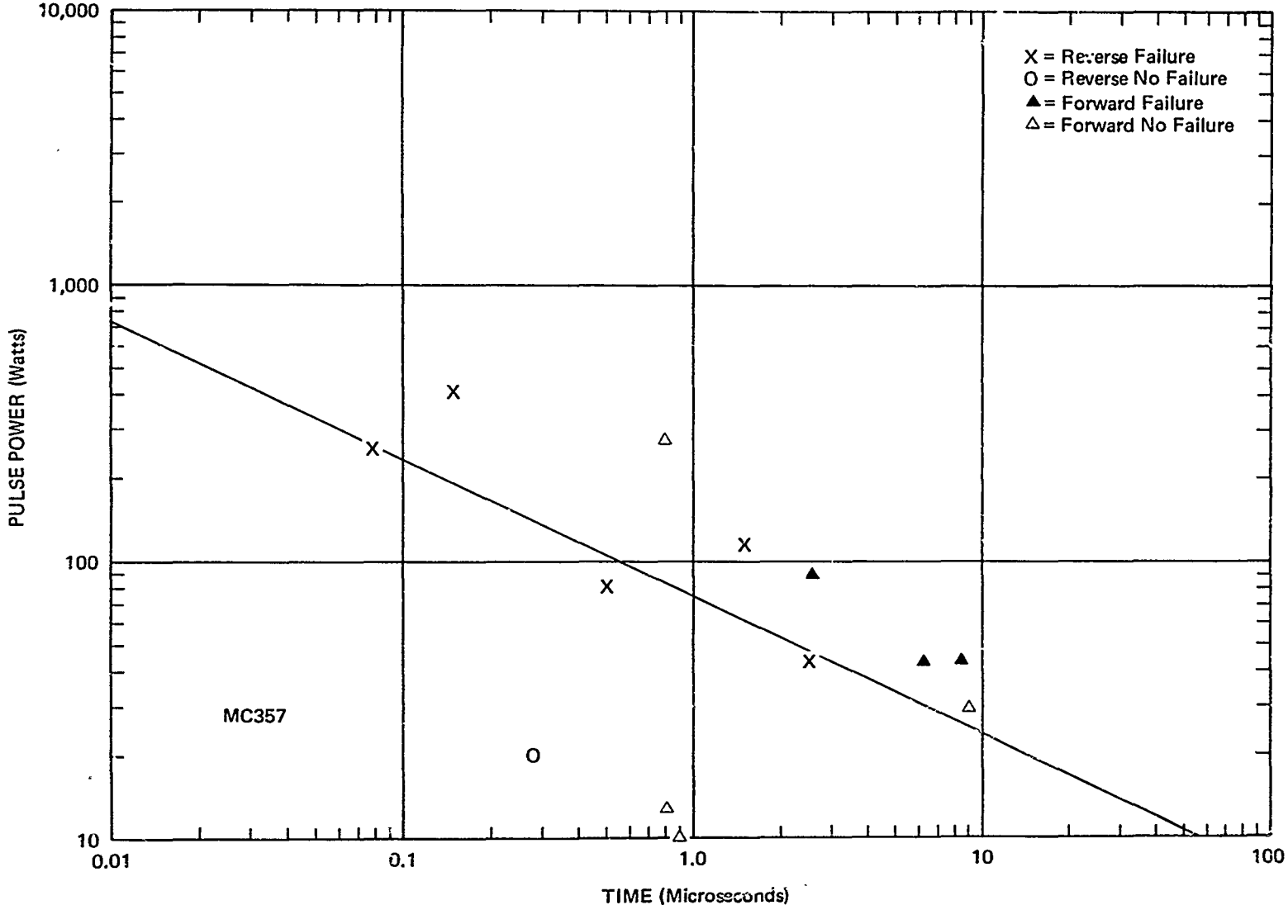
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
G129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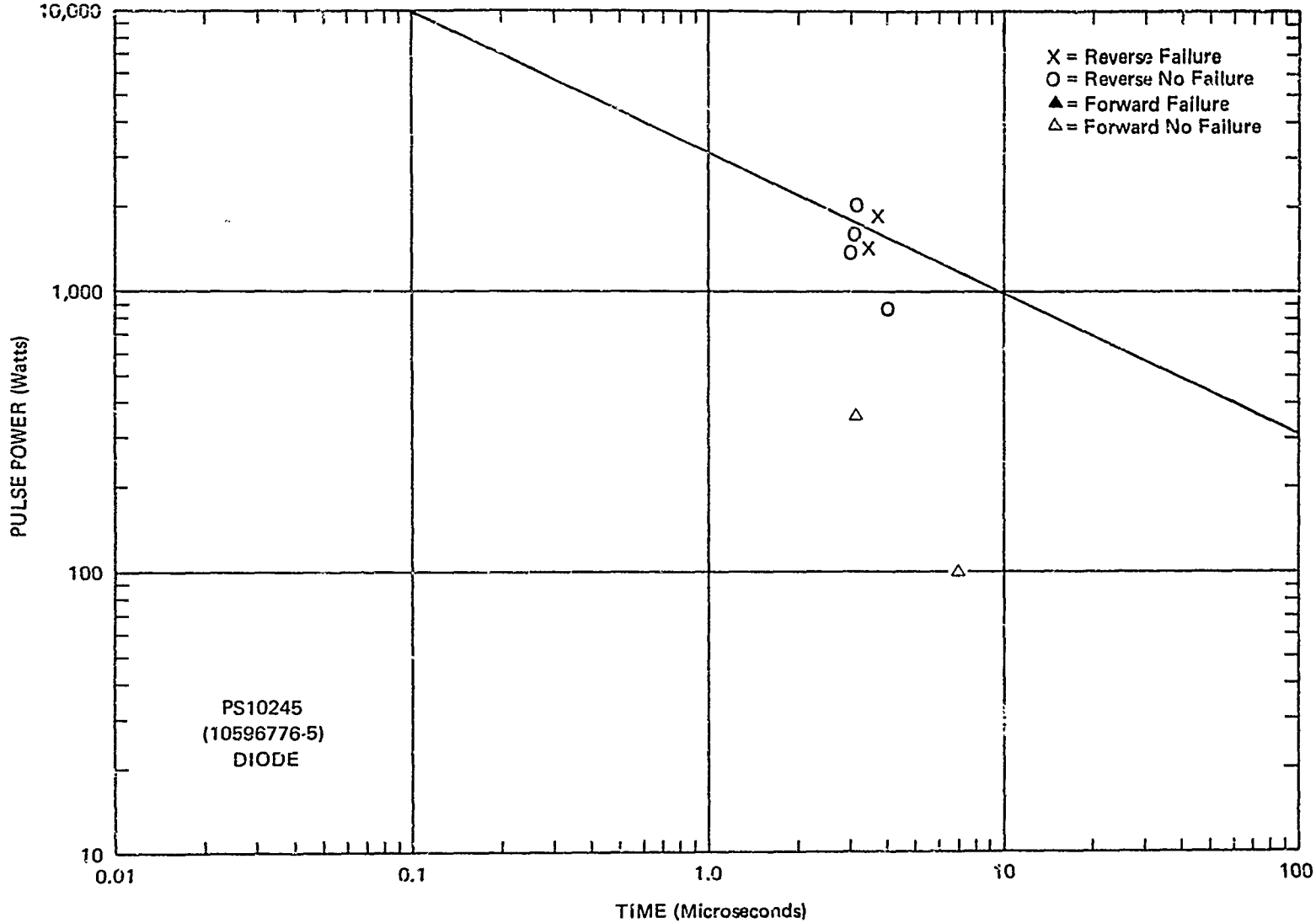
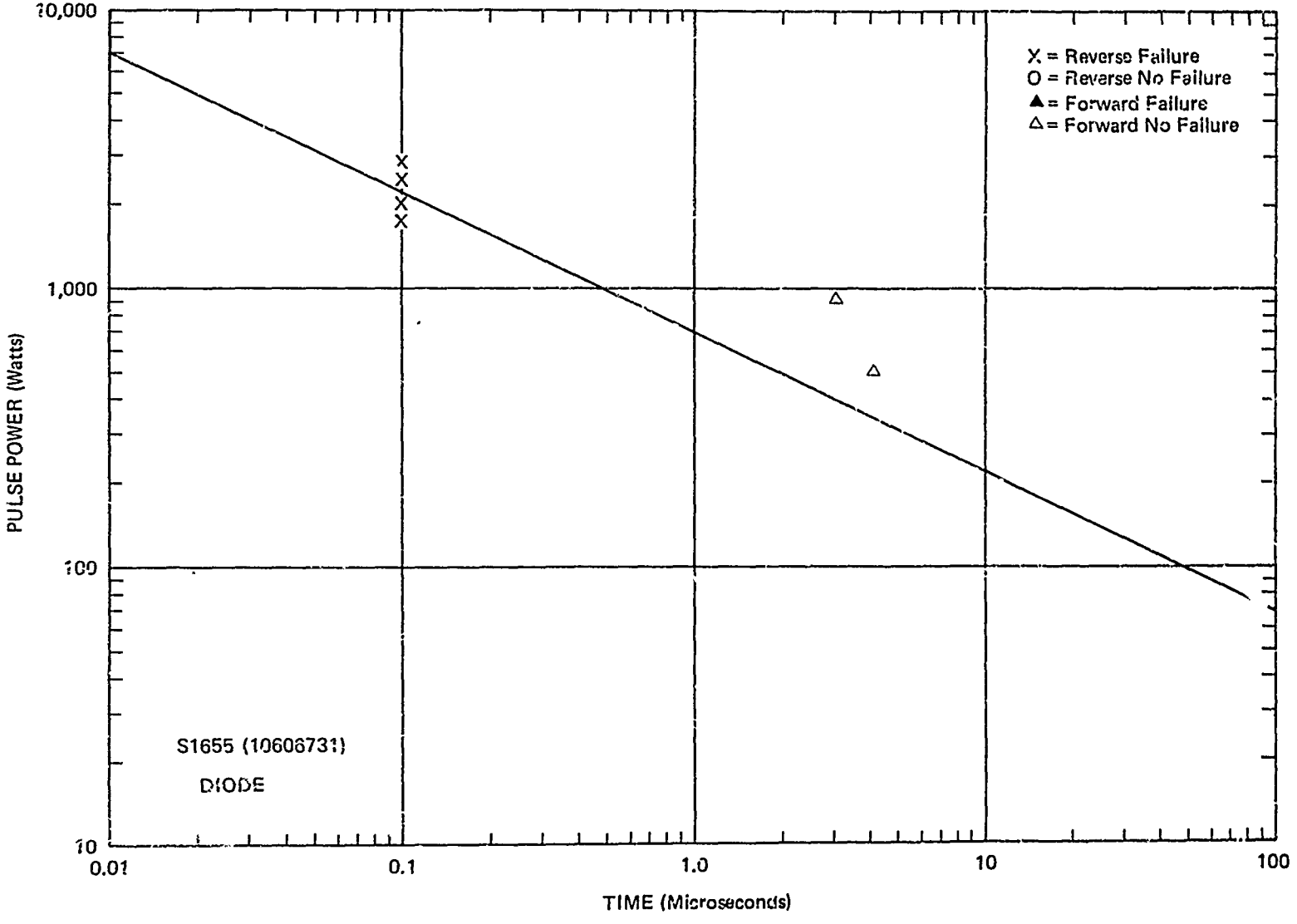
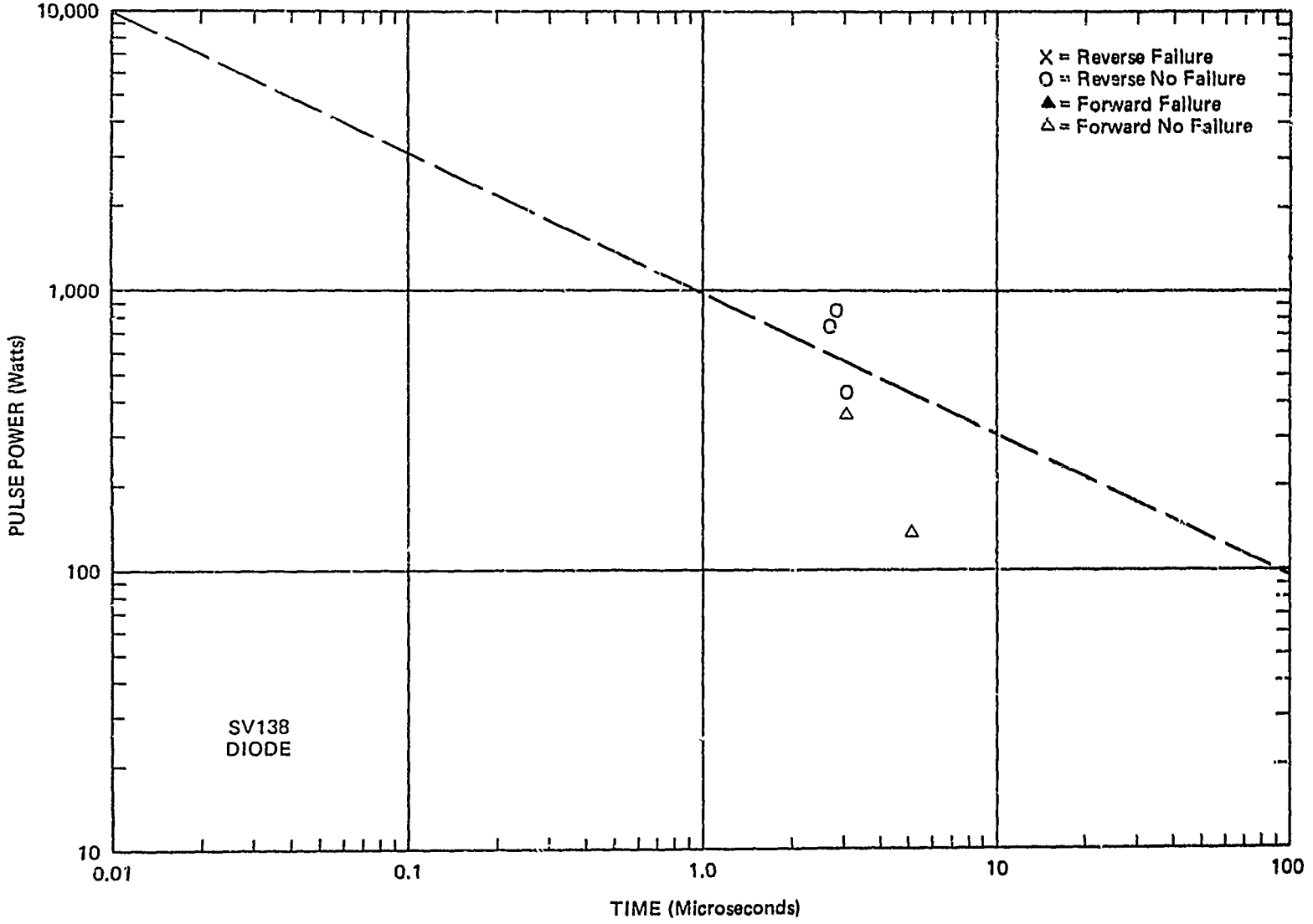
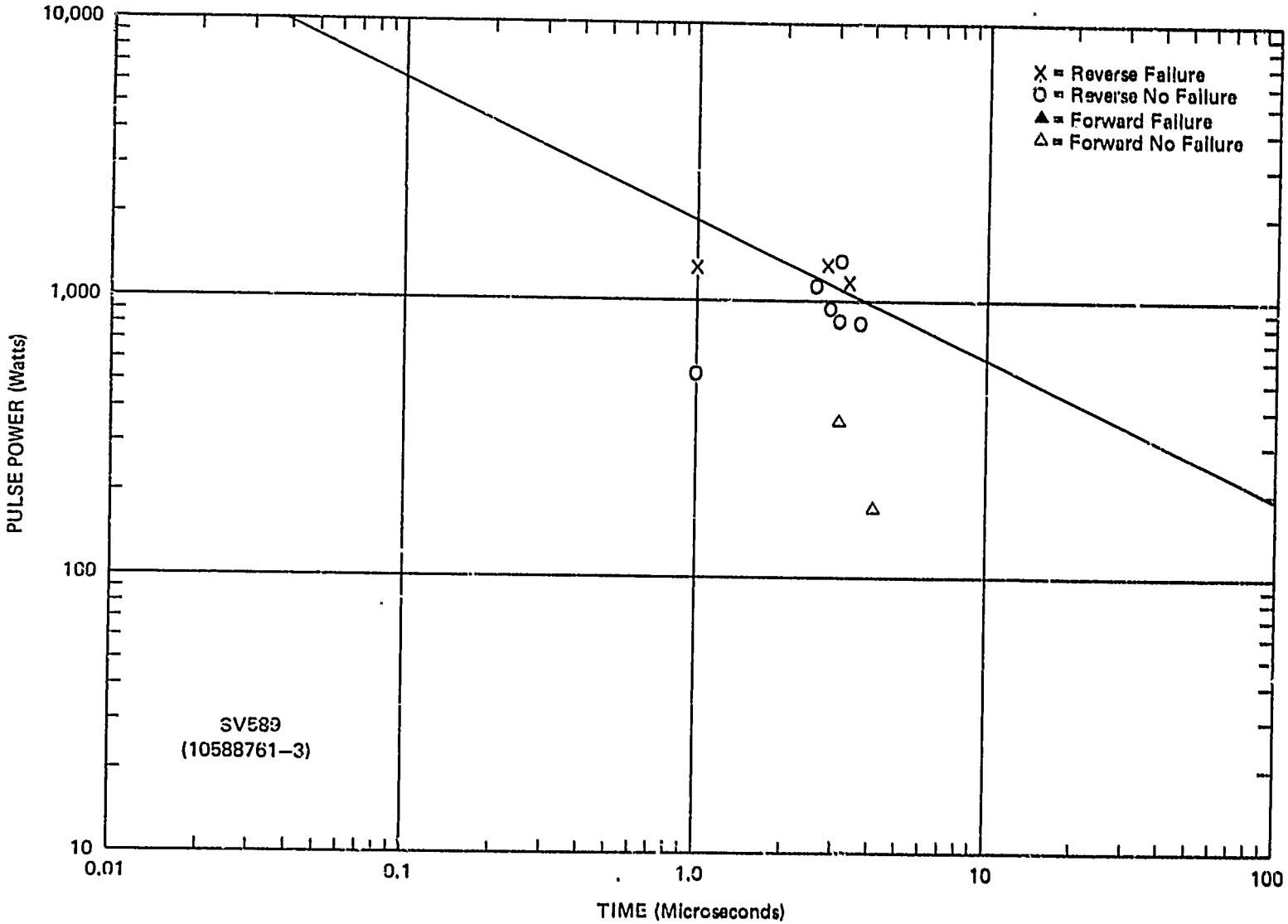
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MC357

3-50

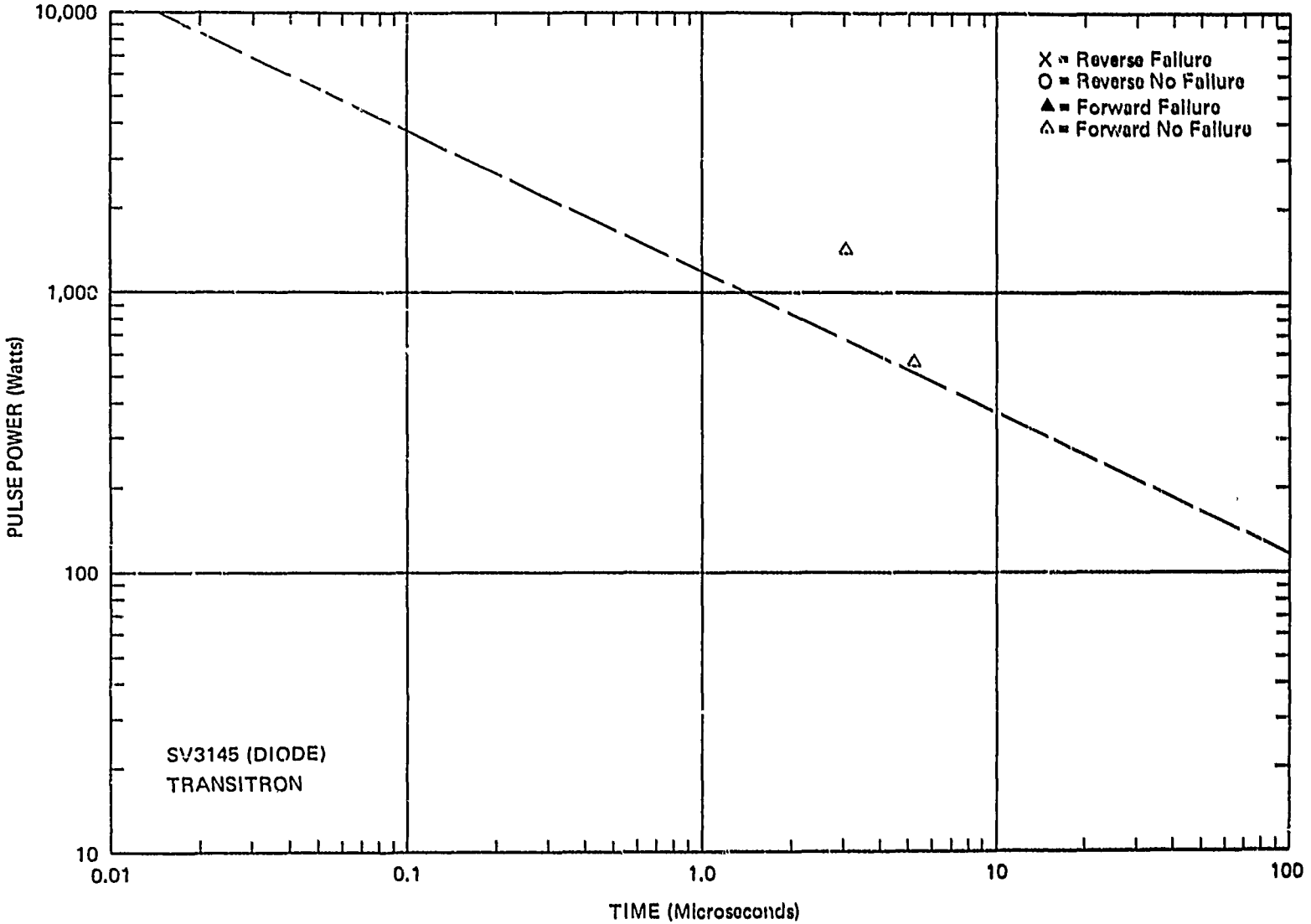

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
PS10245
(10596776-5)
DIODE

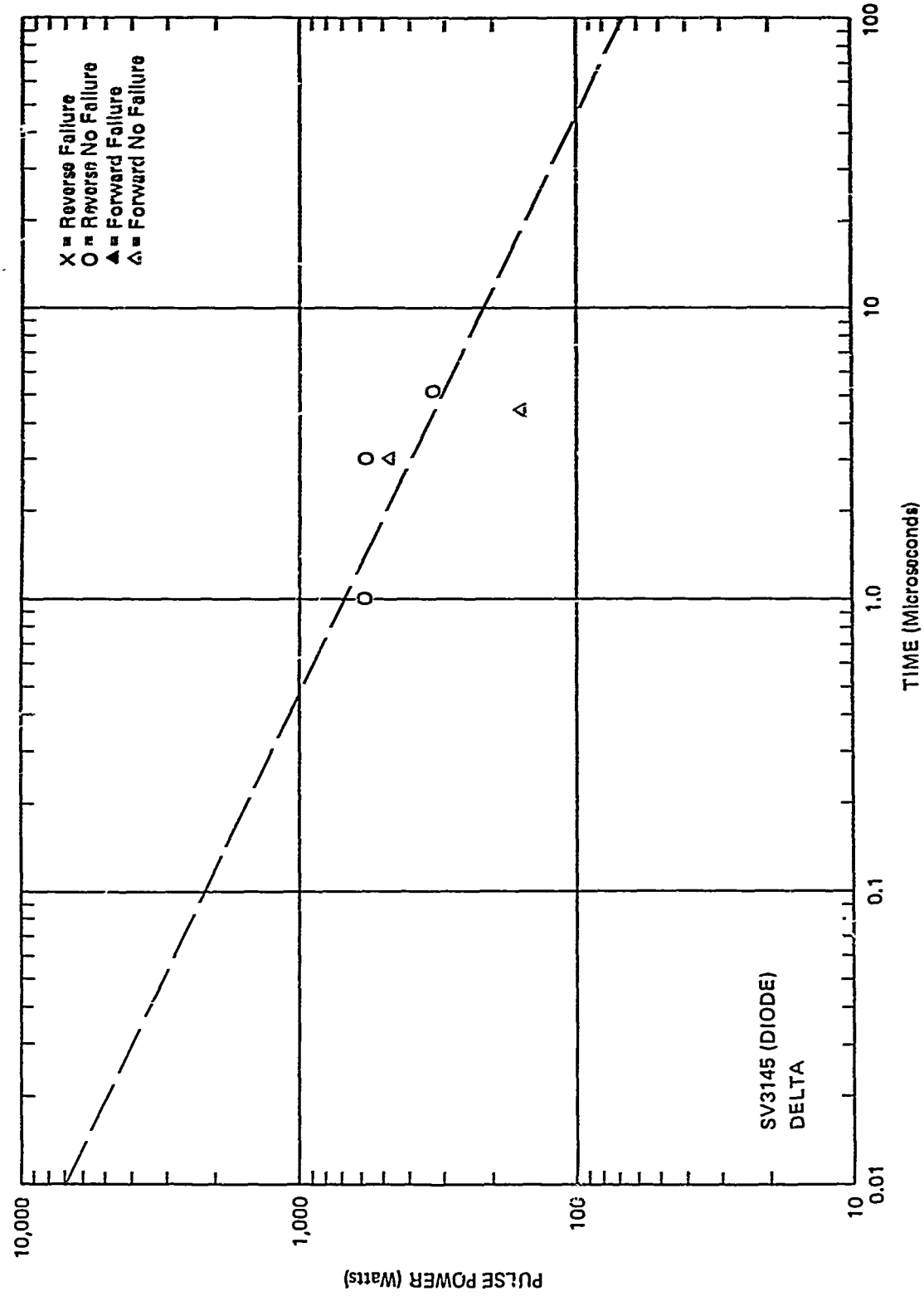

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
S1655 (10606731)
DIODE

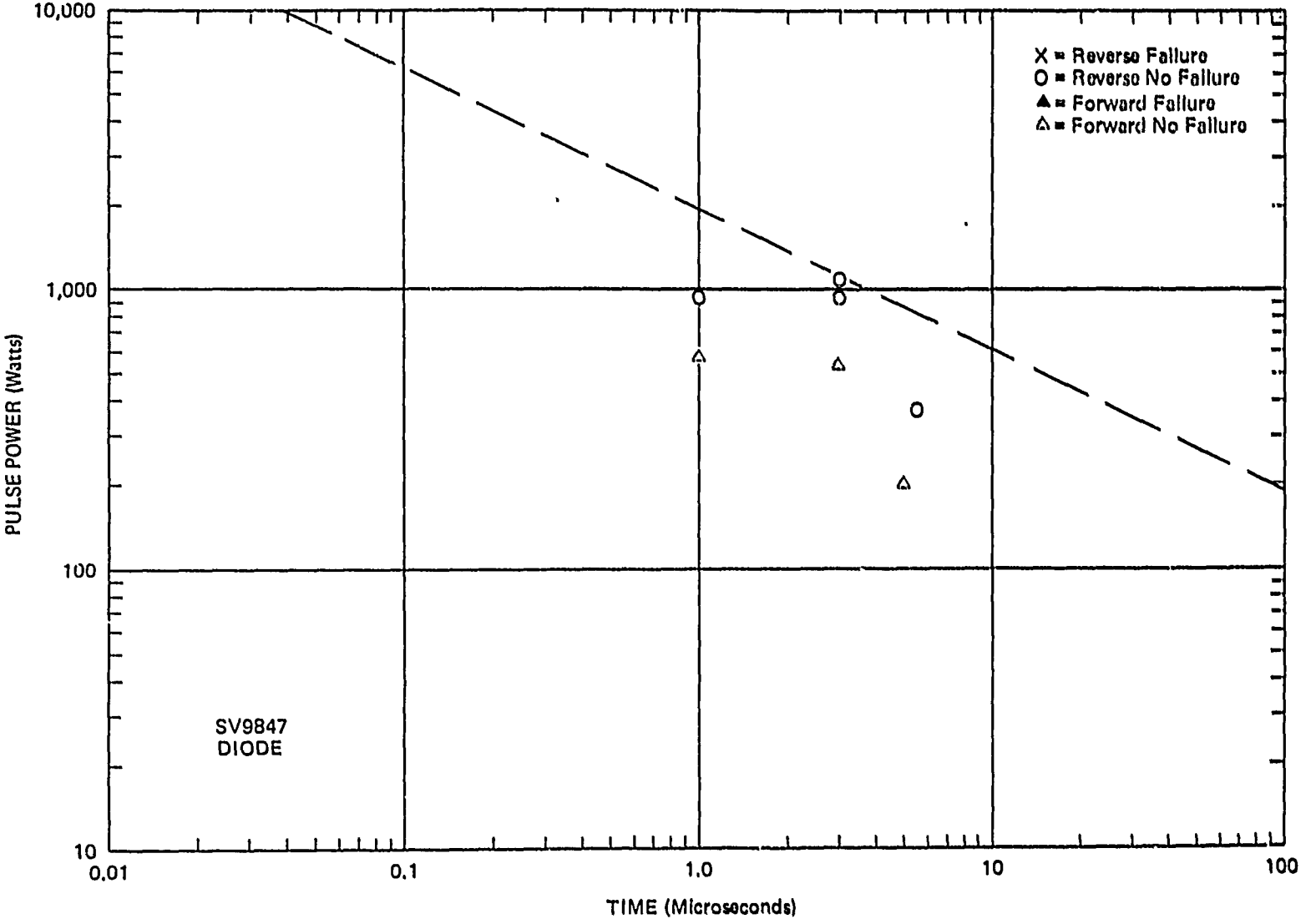

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SV138
DIODE


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SV589
(10588761–3)

3.54

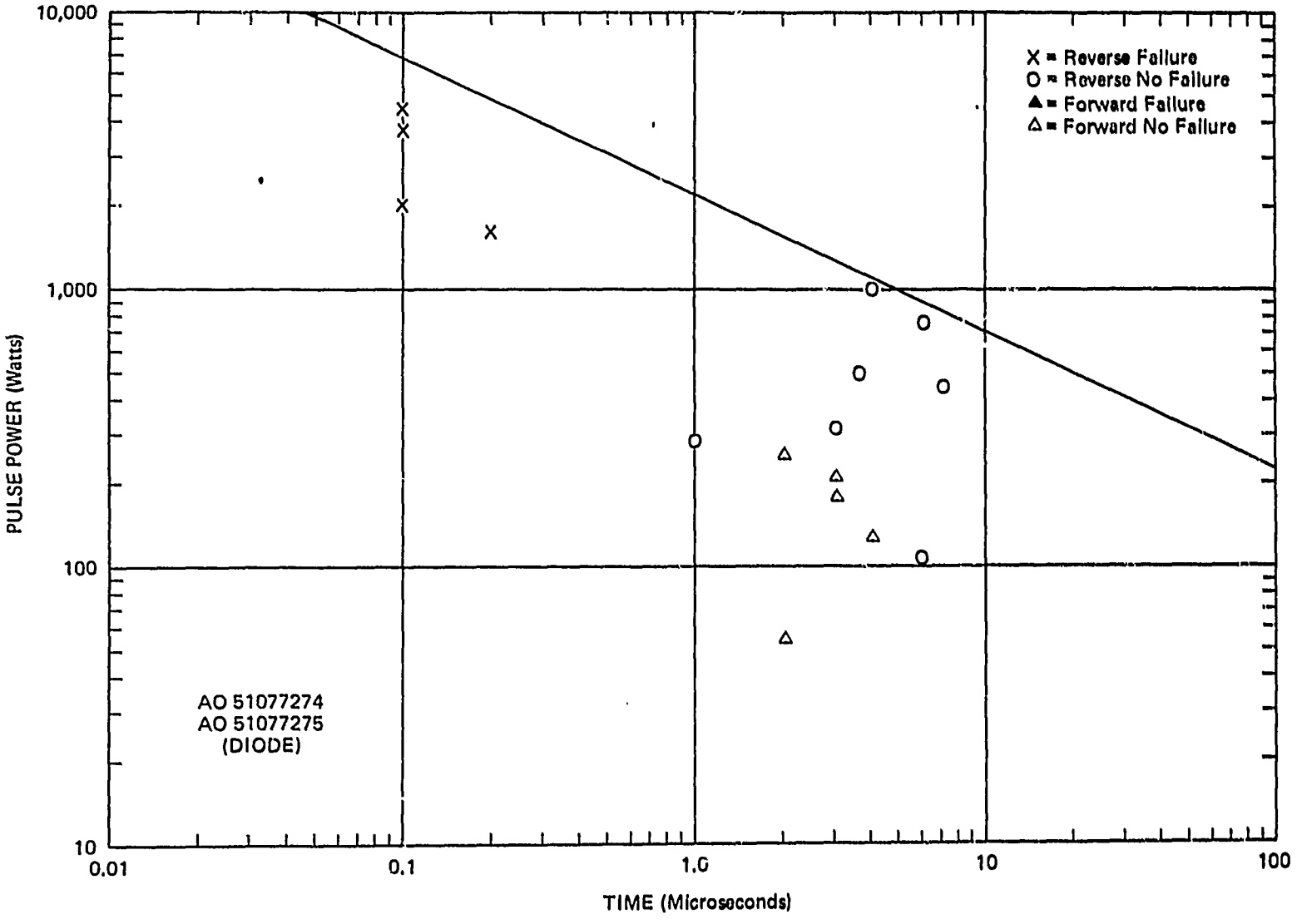

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SV3145 (DIODE)
TRANSITRON

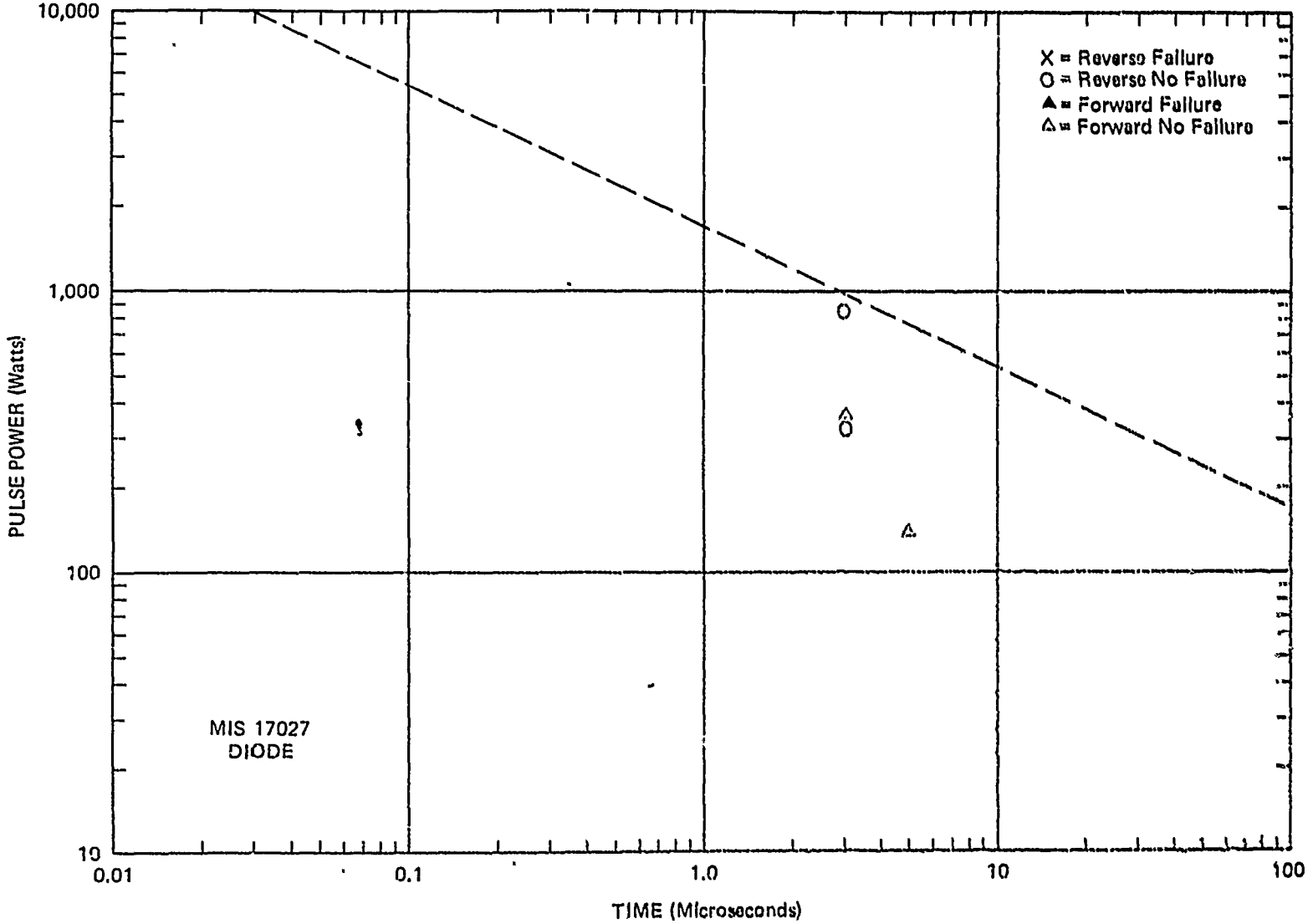

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SV3145 (DIODE)
DELTA
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

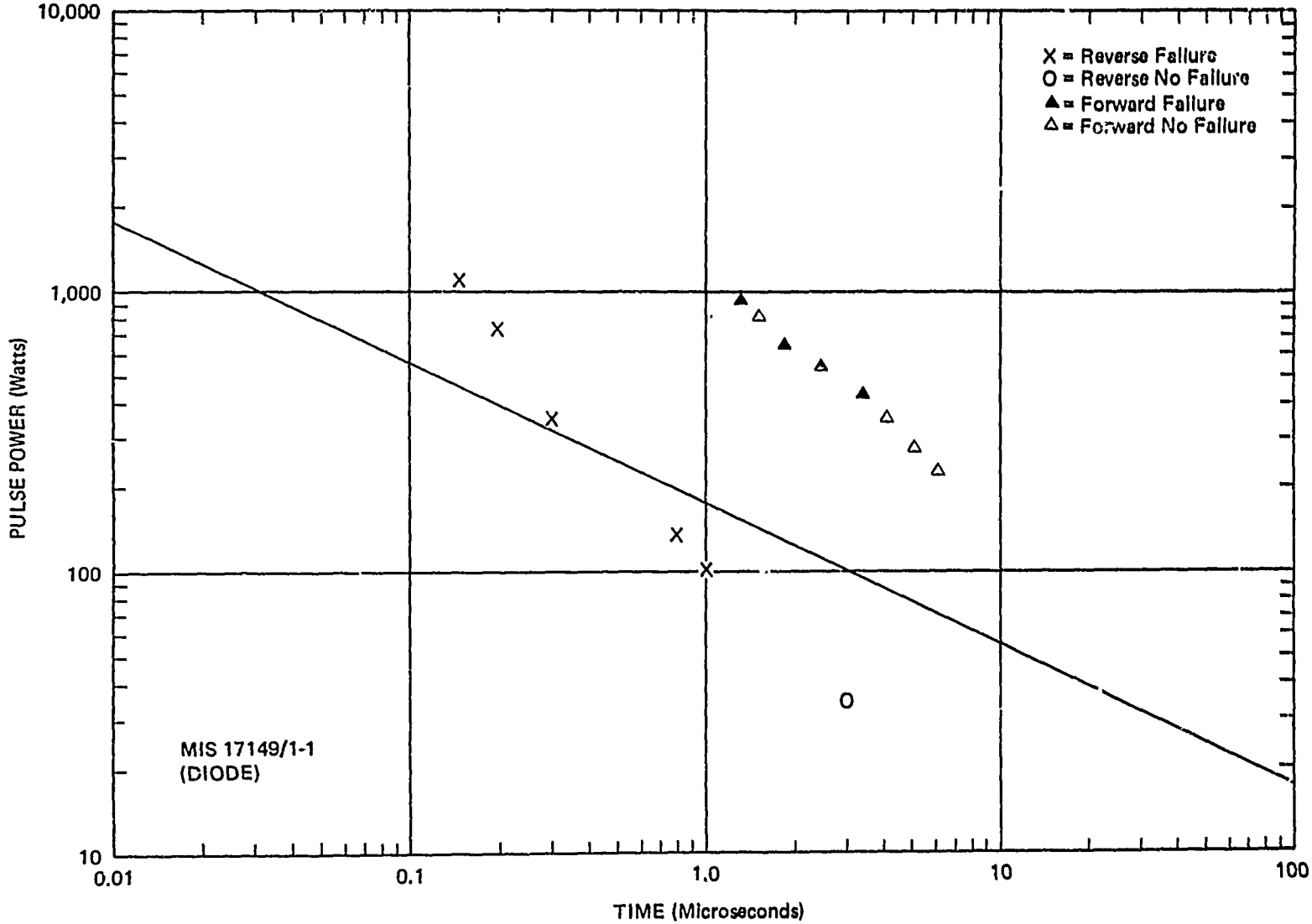

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SV9847
DIODE

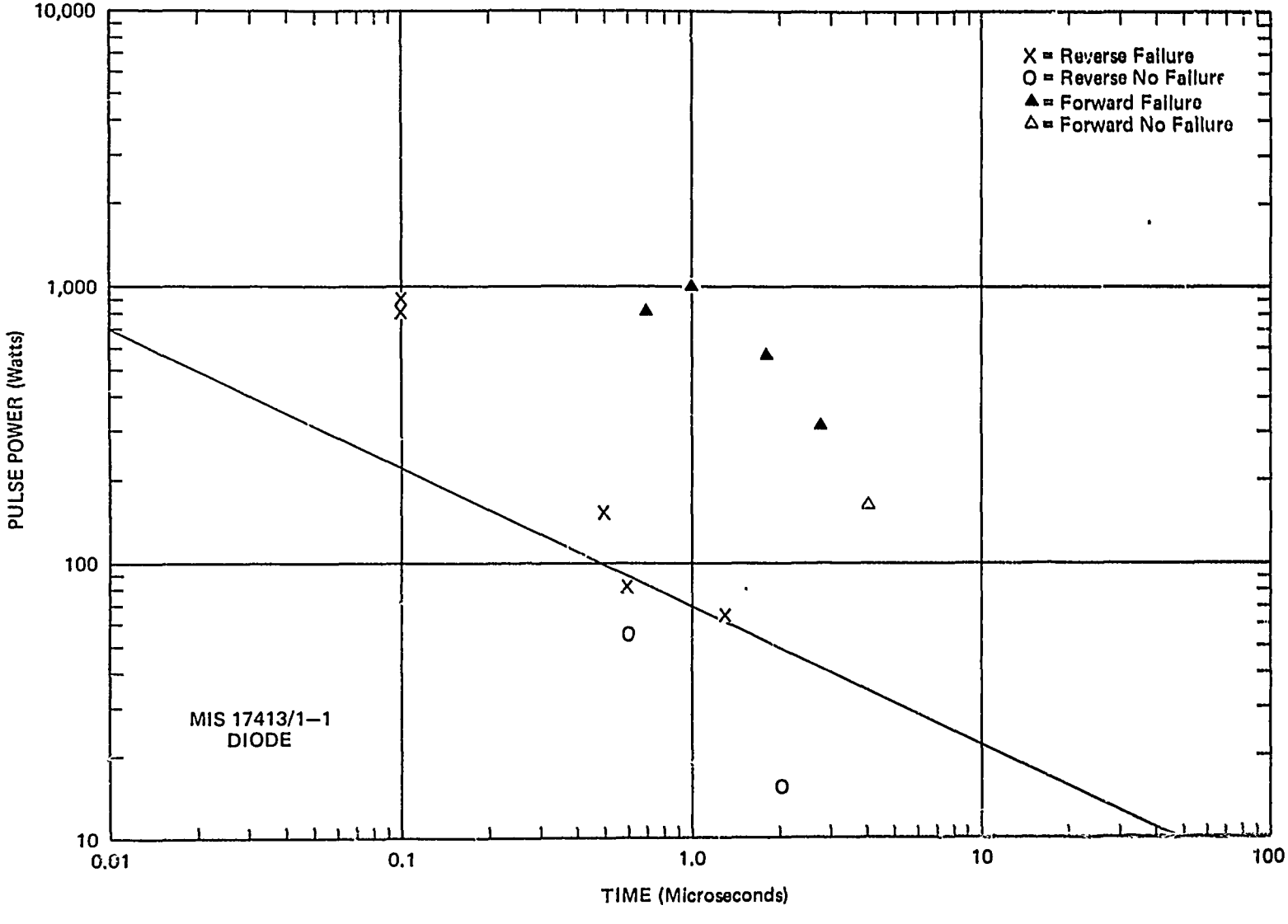
3.57

K' = 1.9


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
AO 51077274
AO 51077275
(DIODE)

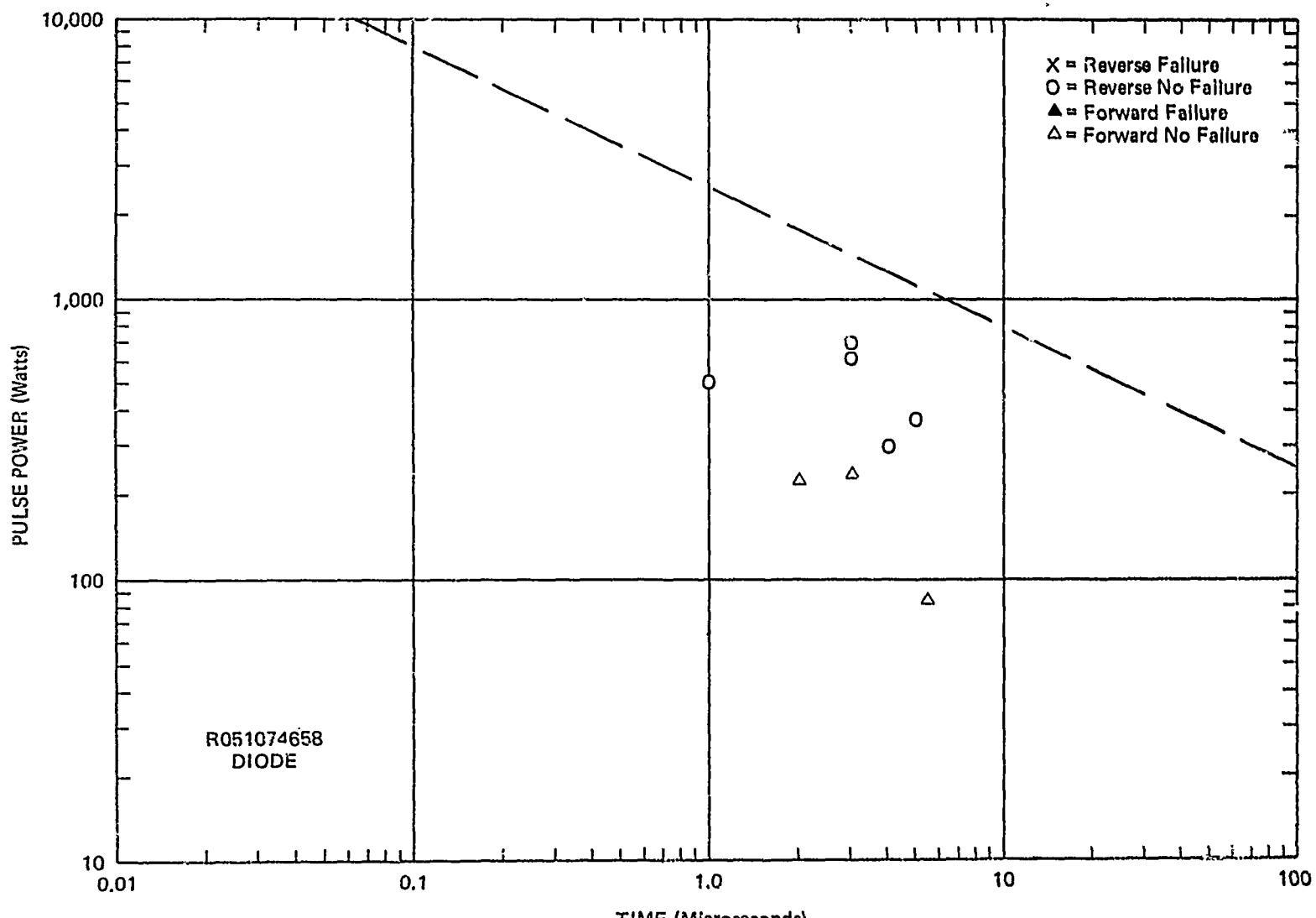

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17027
DIODE


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17149/1-1
(DIODE)


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17413/1–1
DIODE

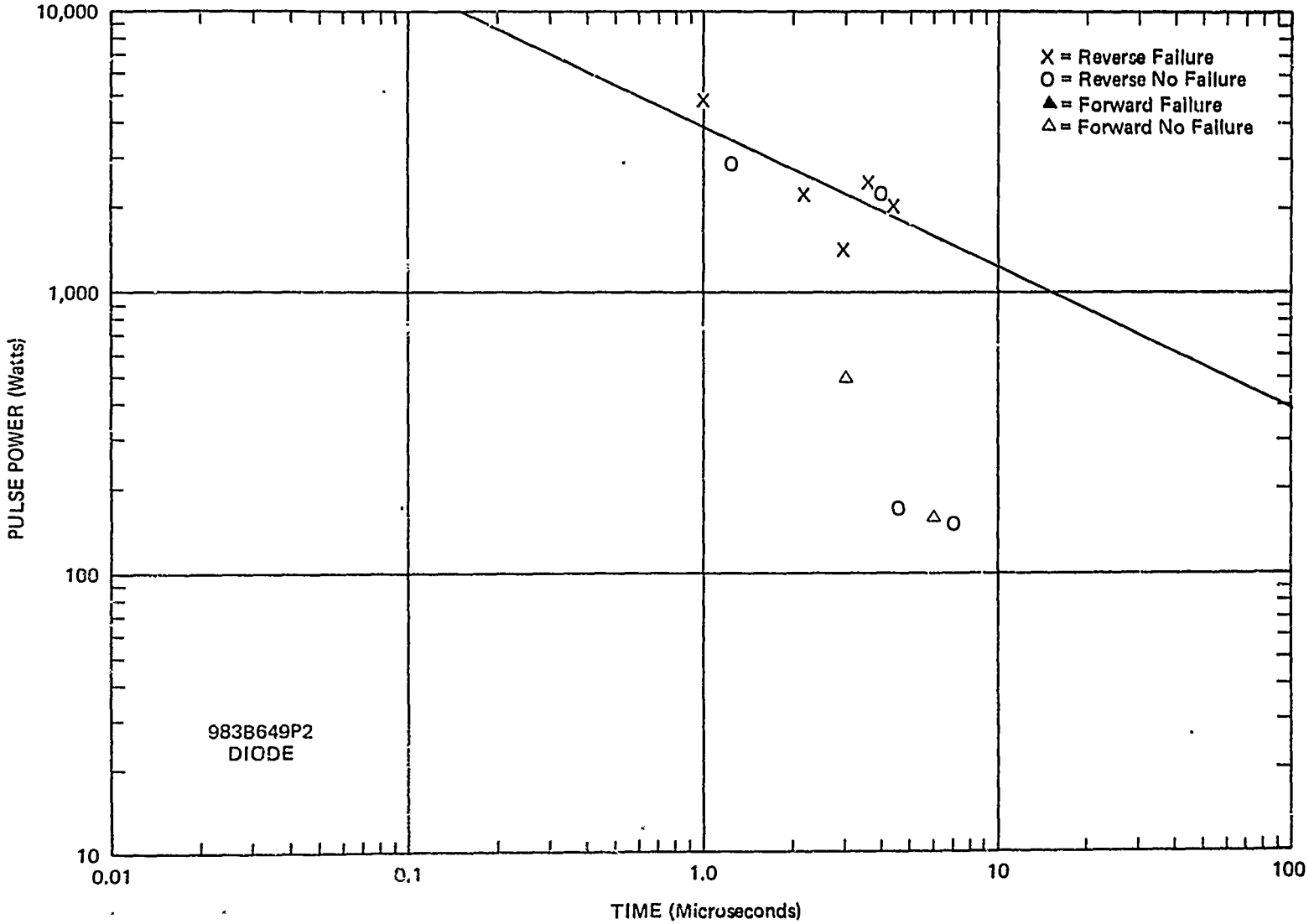
3.61

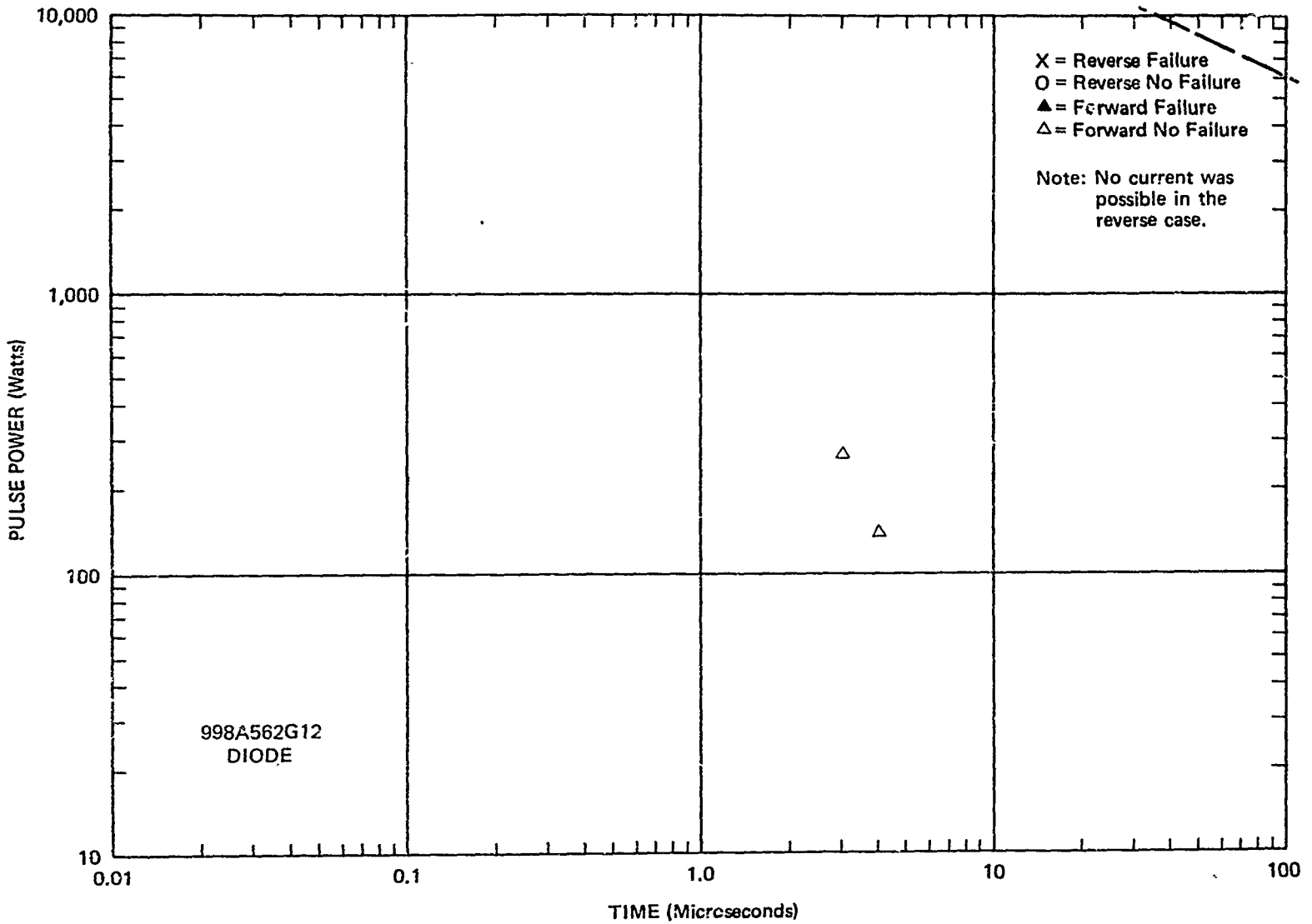
K' = .070

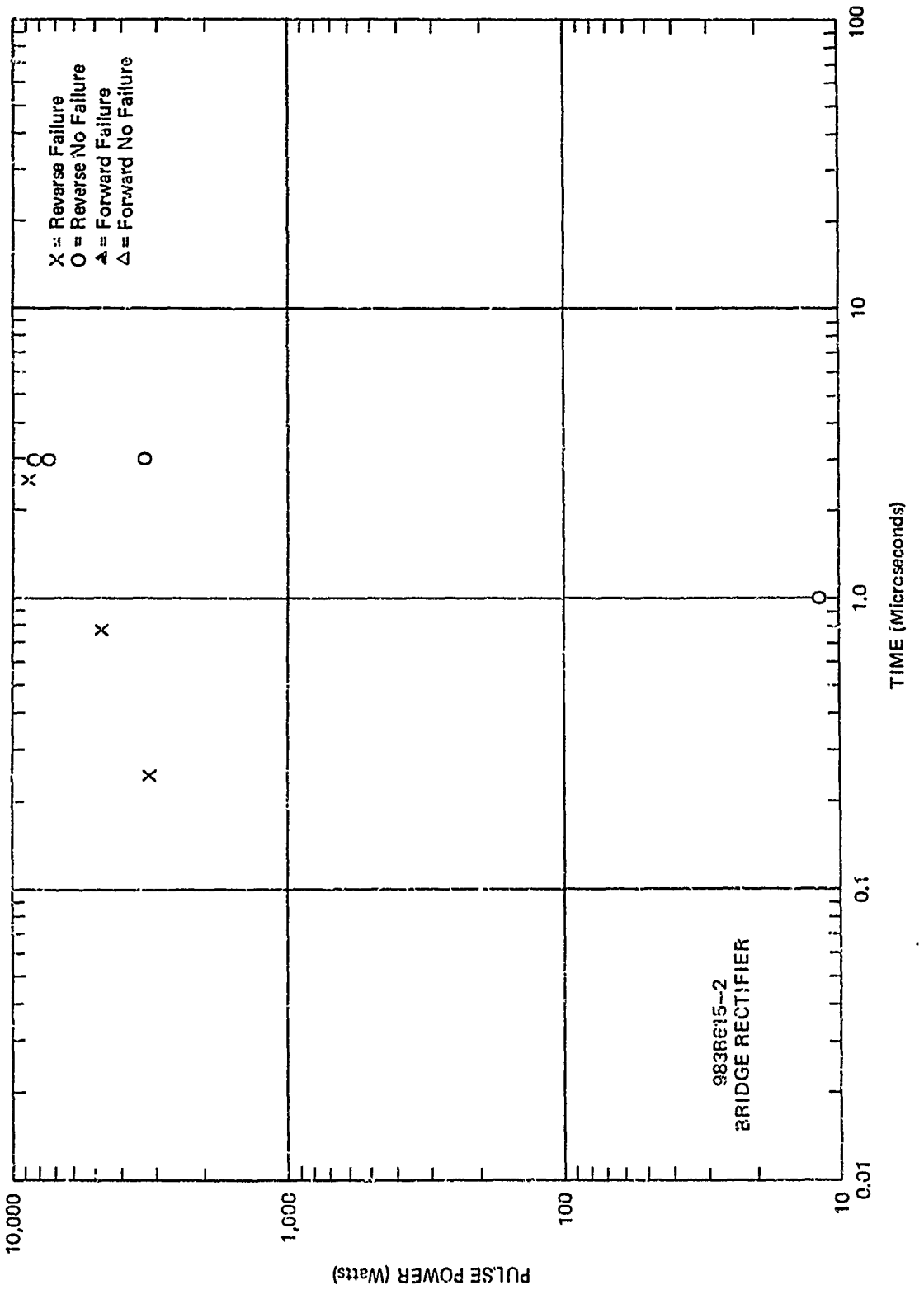

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
R051074658
DIODE

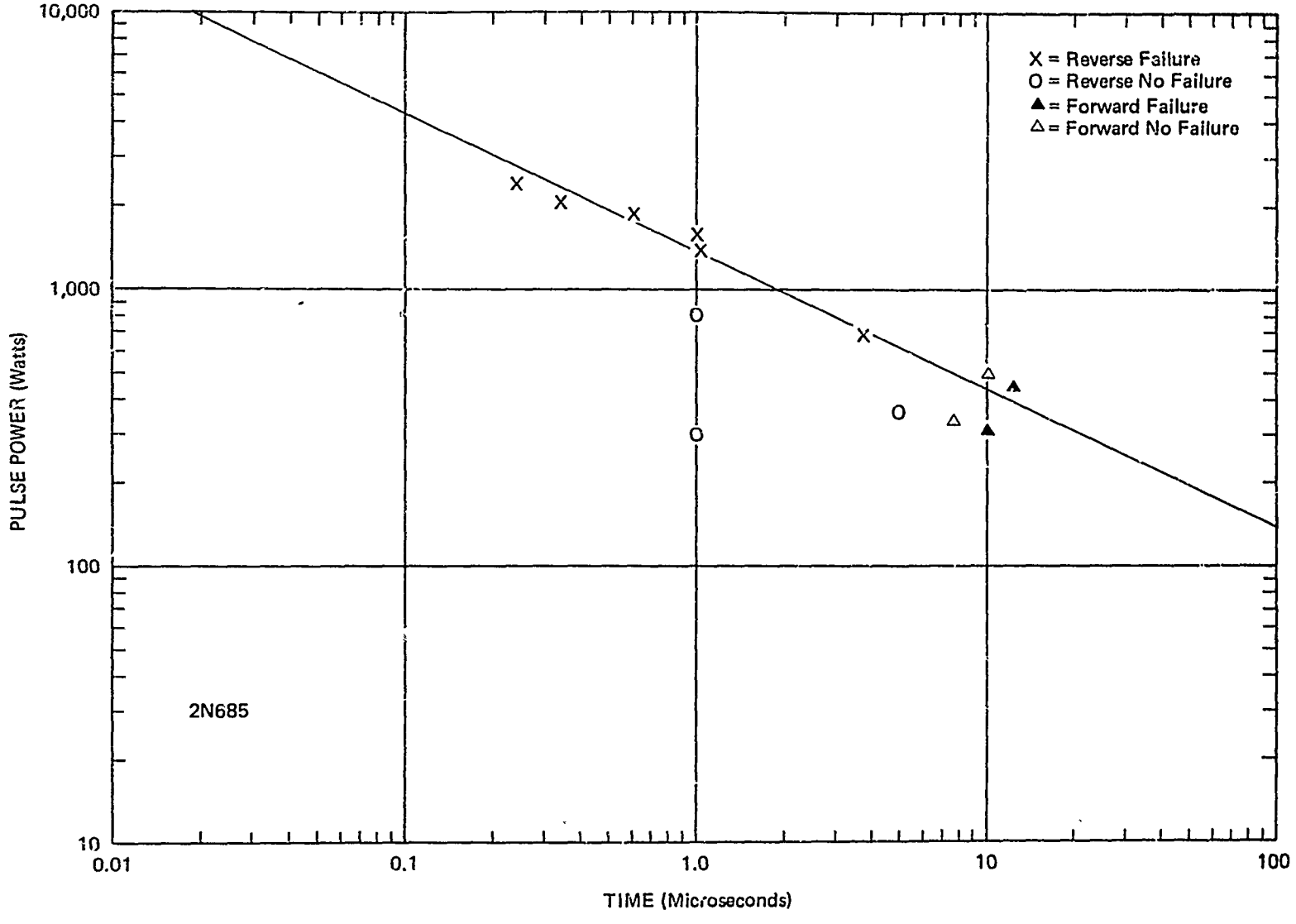
3.62

K' = 2.5

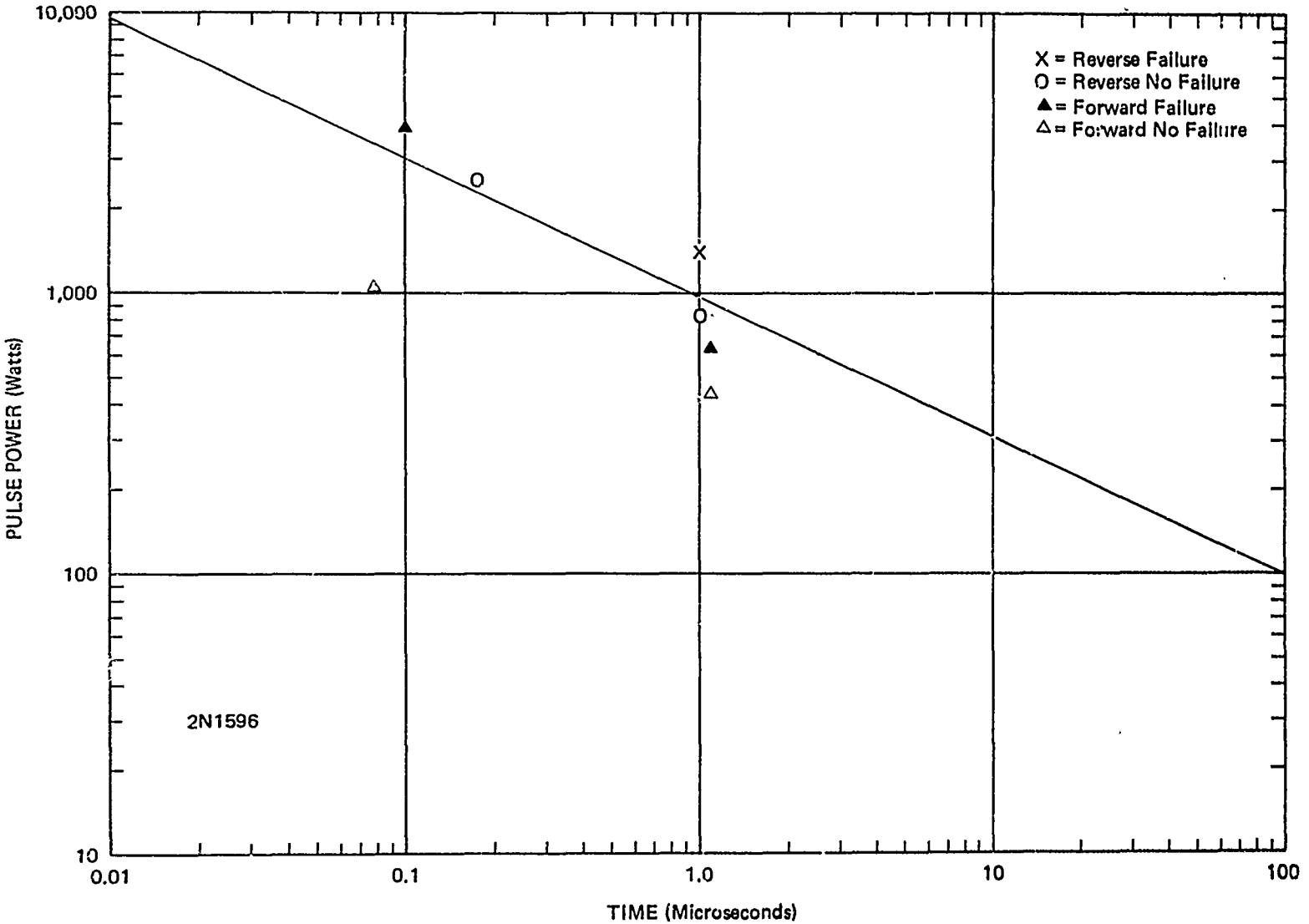

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
983B649P2
DIODE


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
Note: No current was possible in the reverse case.
998A562G12
DIODE

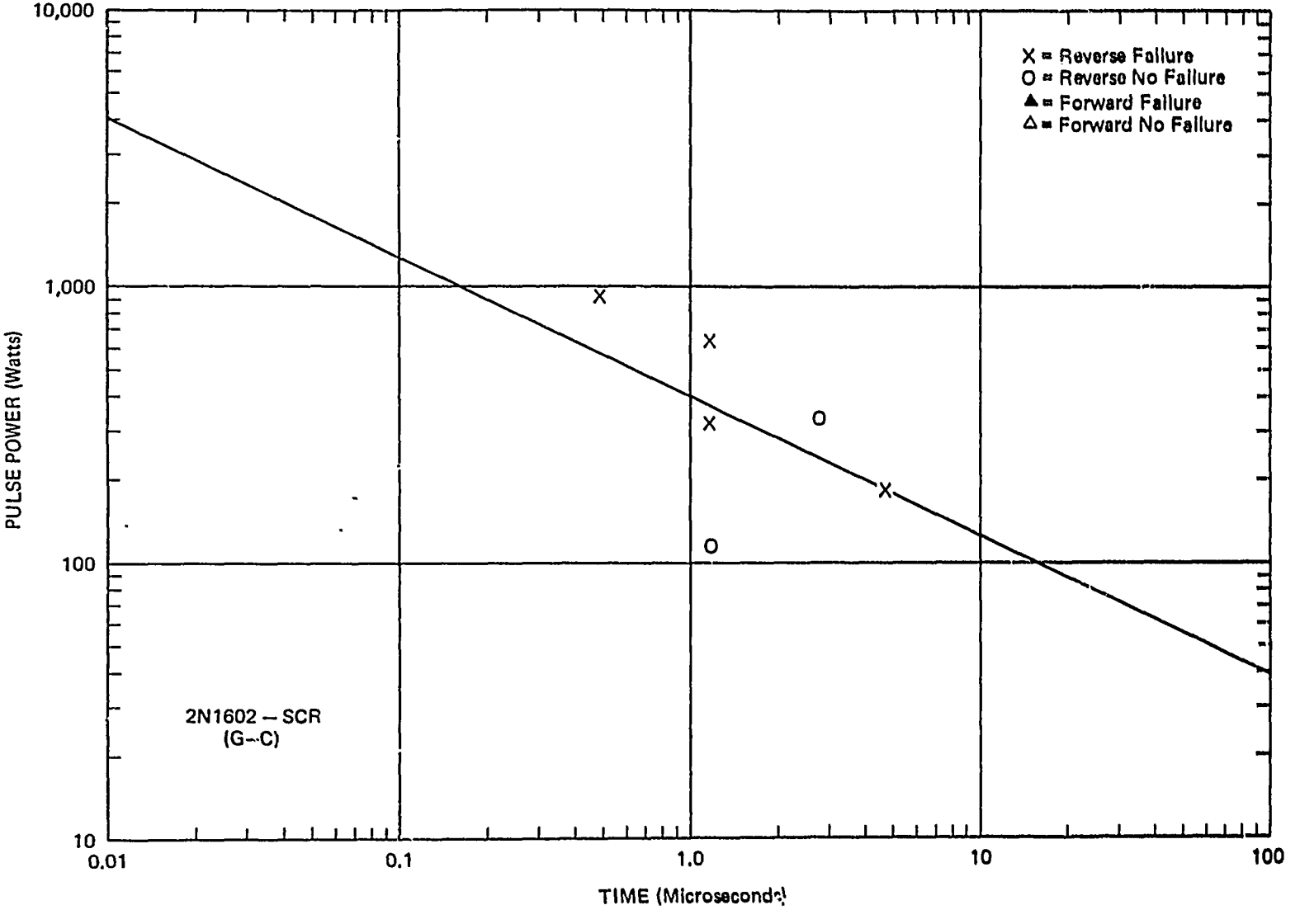

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
983615-2
BRIDGE RECTIFIER
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

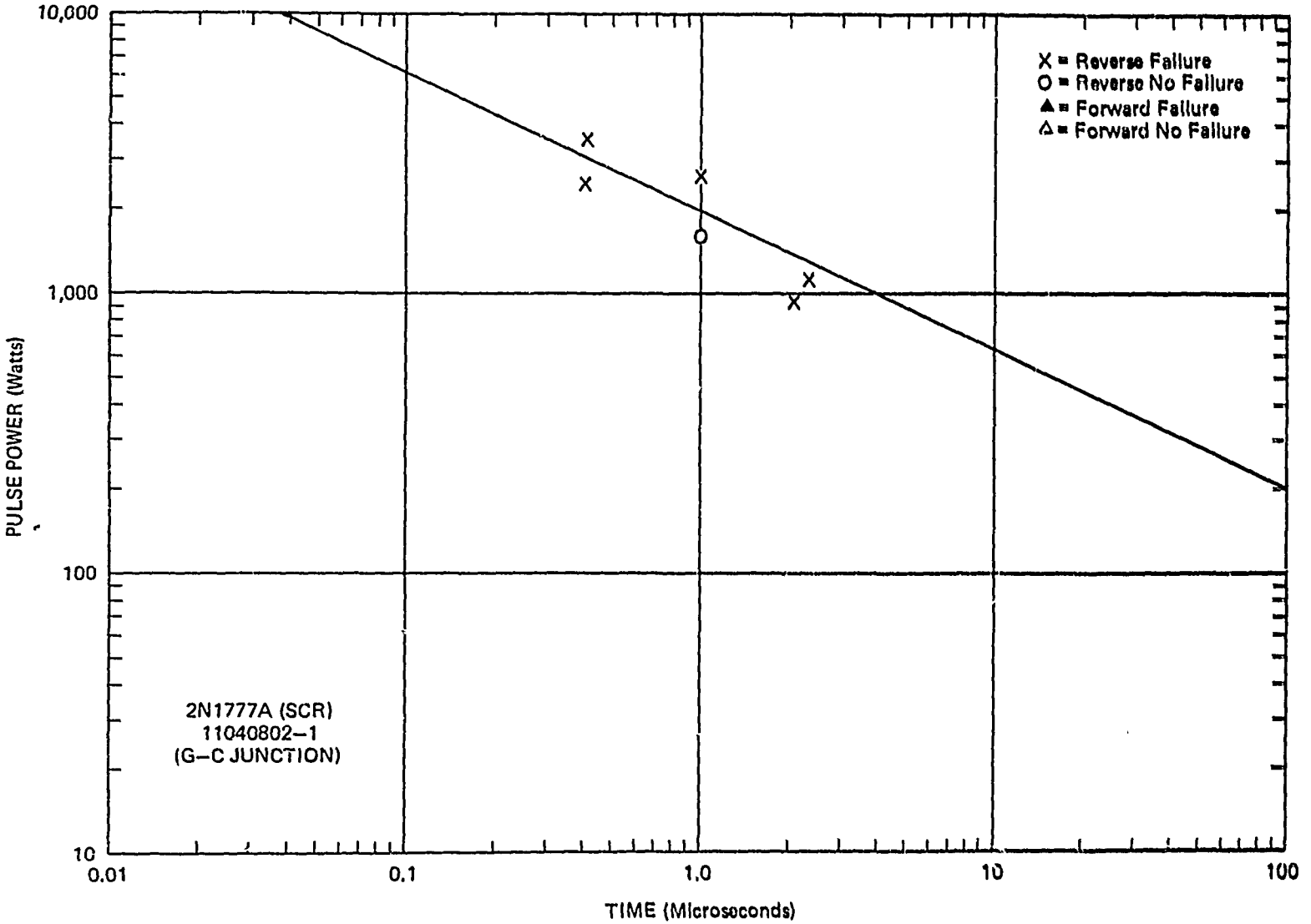

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N685

3.66

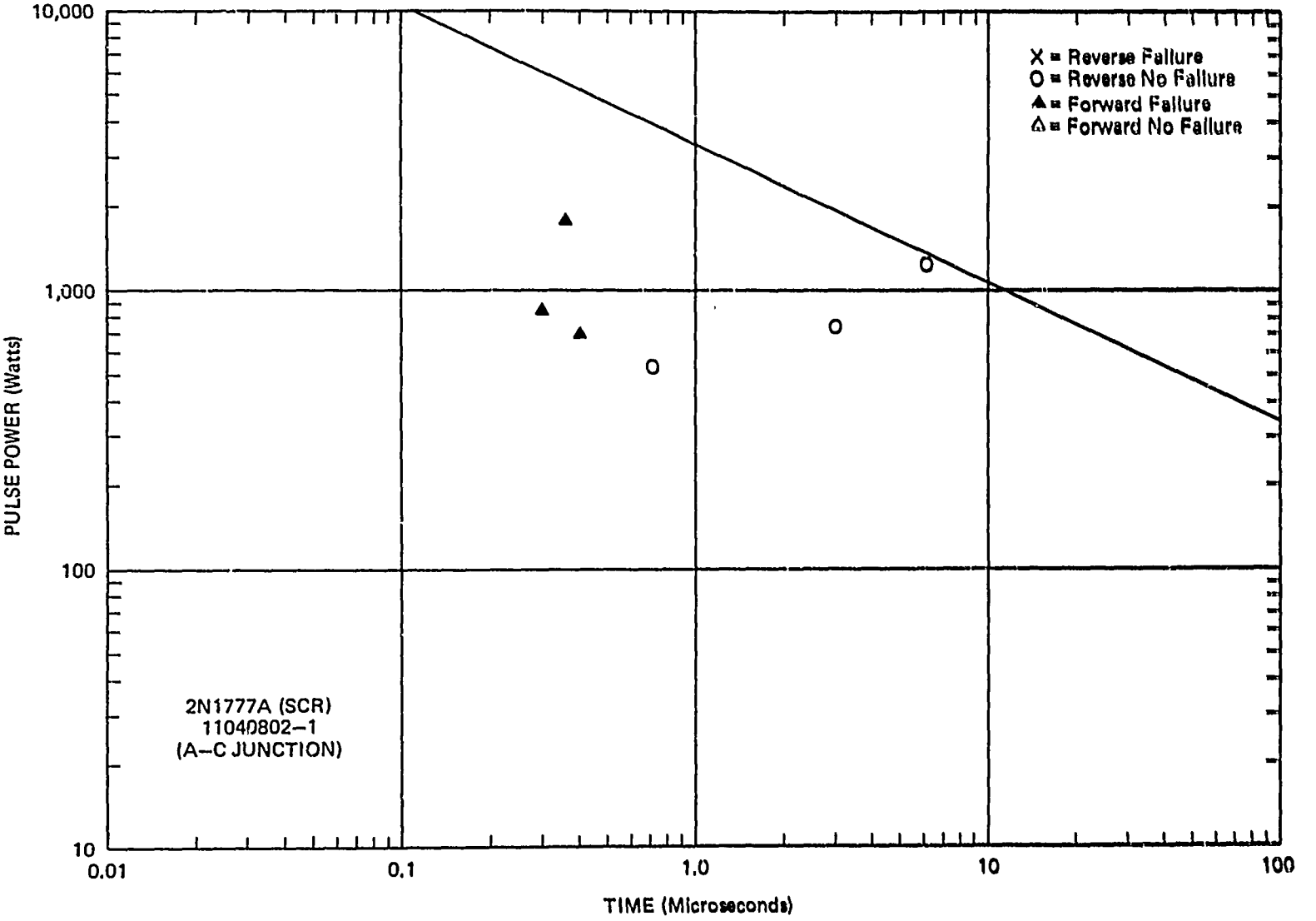

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1596

3.67

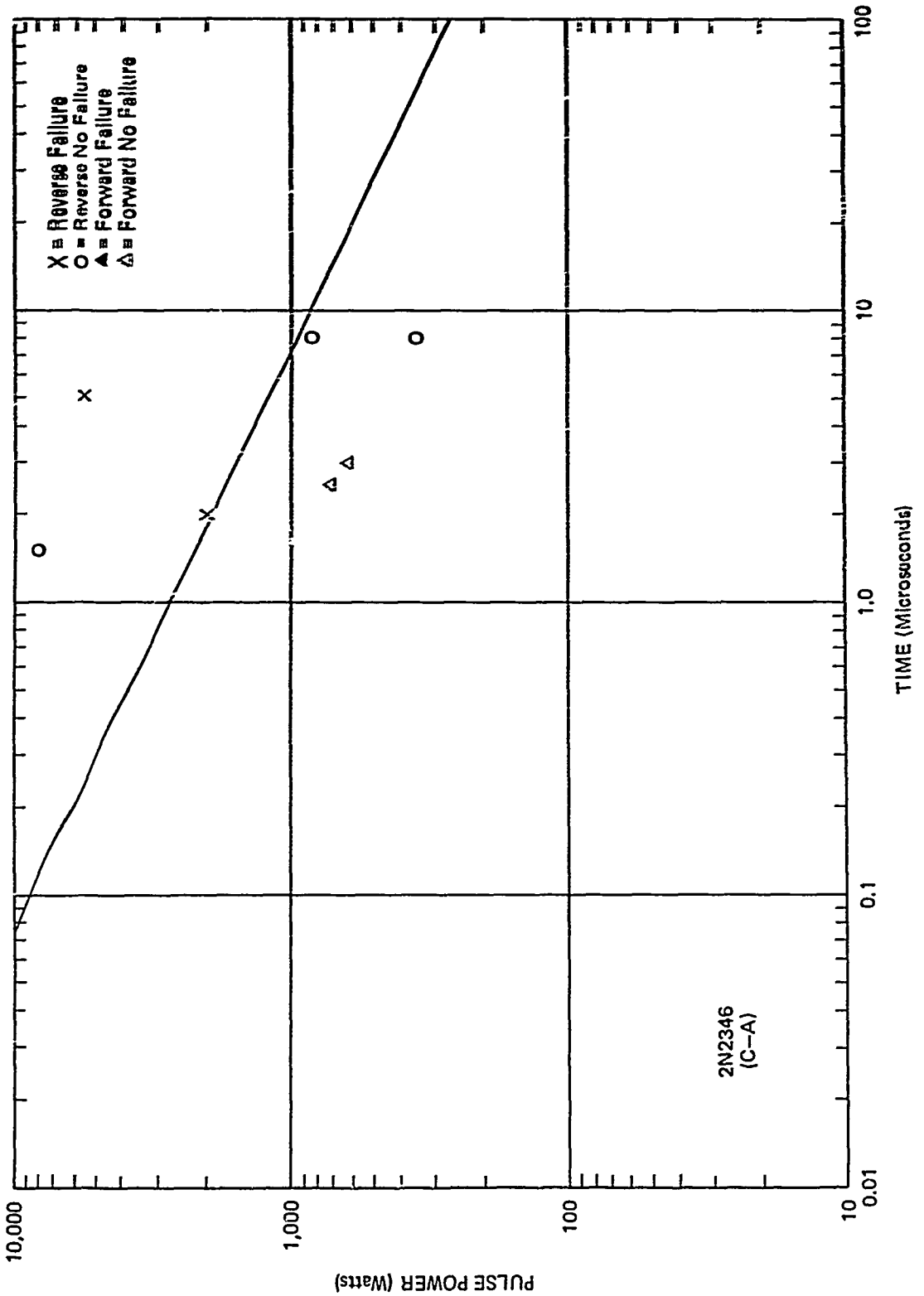

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1602 – SCR
(G–C)

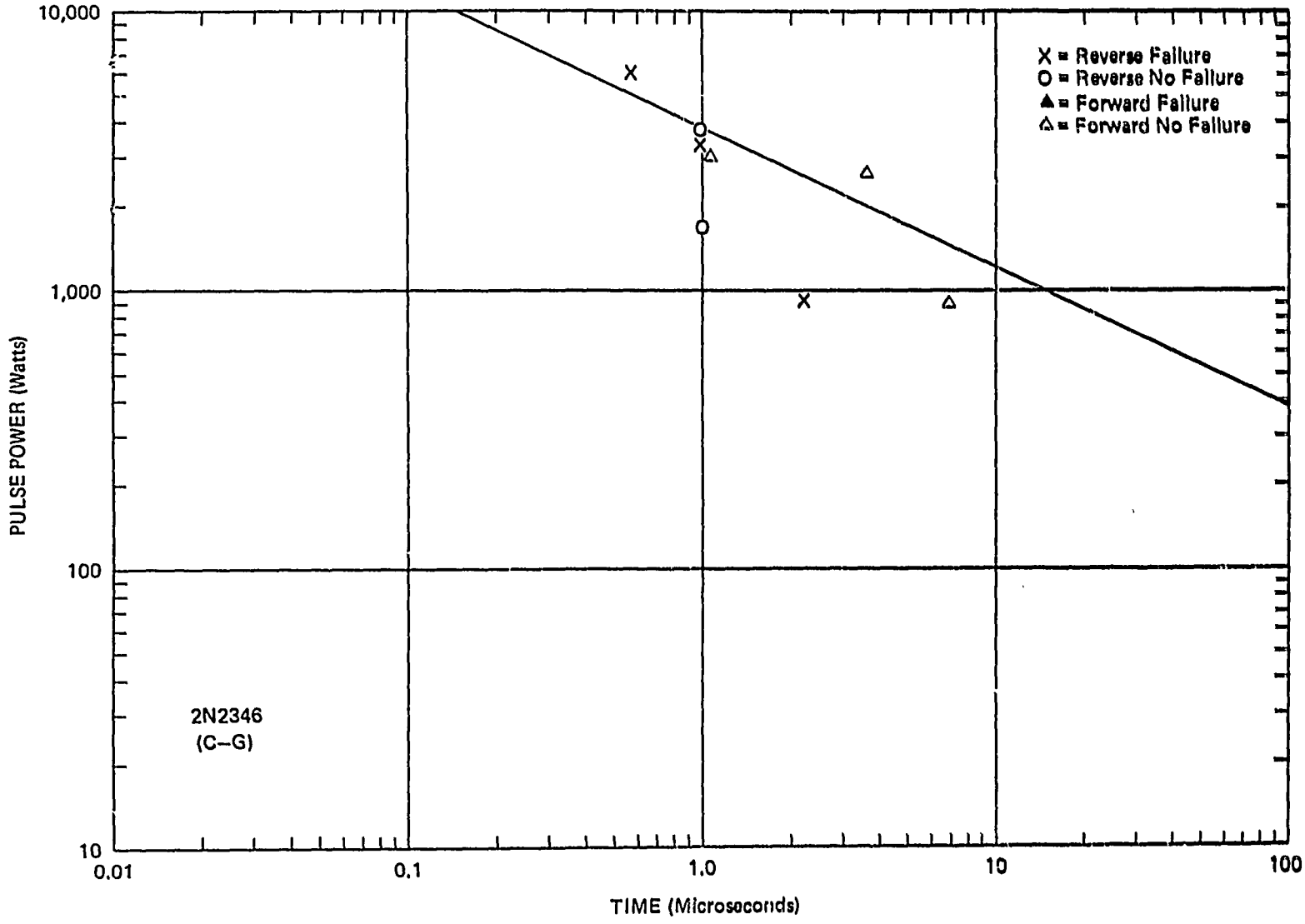

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1777A (SCR)
11040802-1
(G-C JUNCTION)

3.69

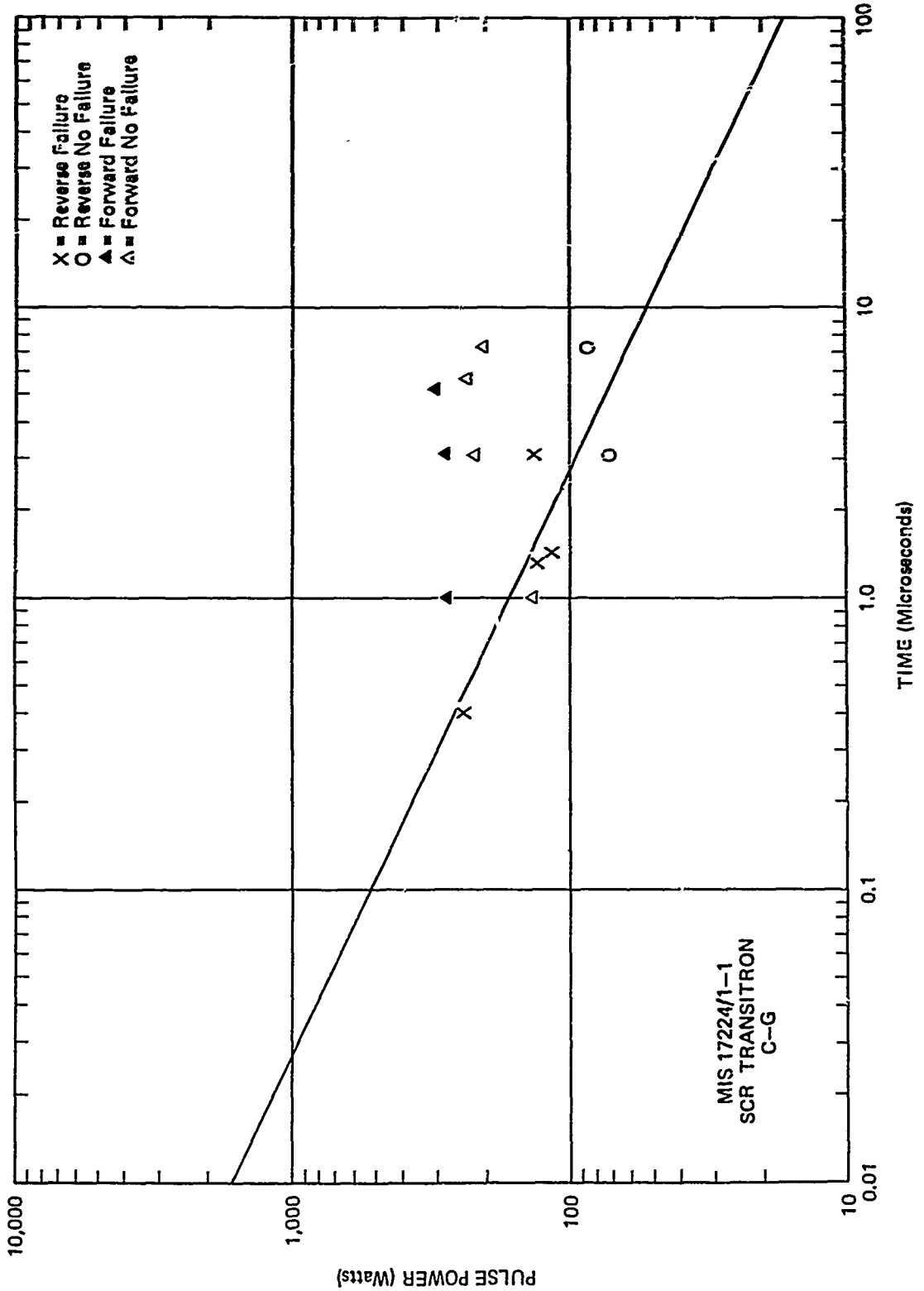

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1777A (SCR)
11040802–1
(A–C JUNCTION)

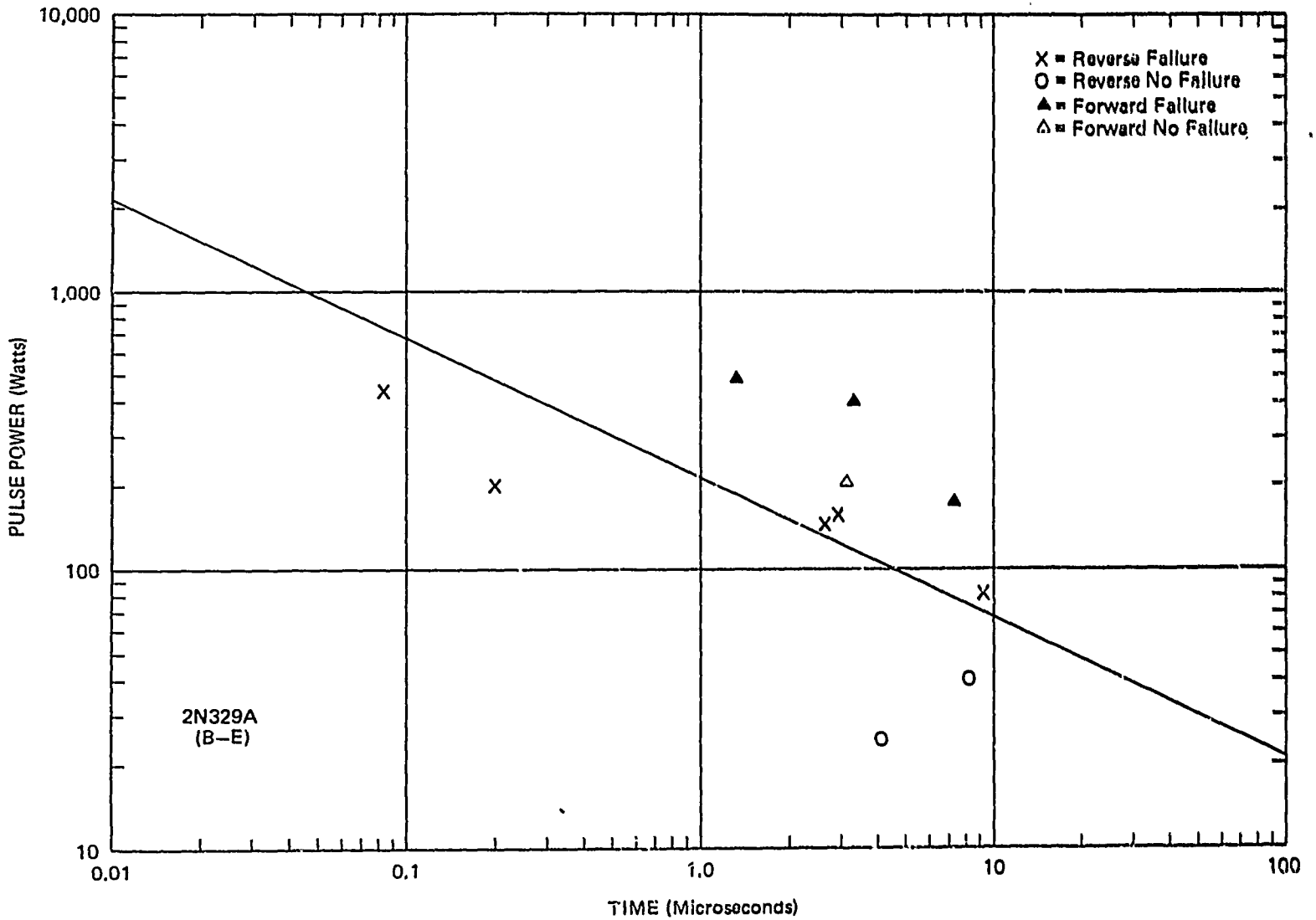
3.70

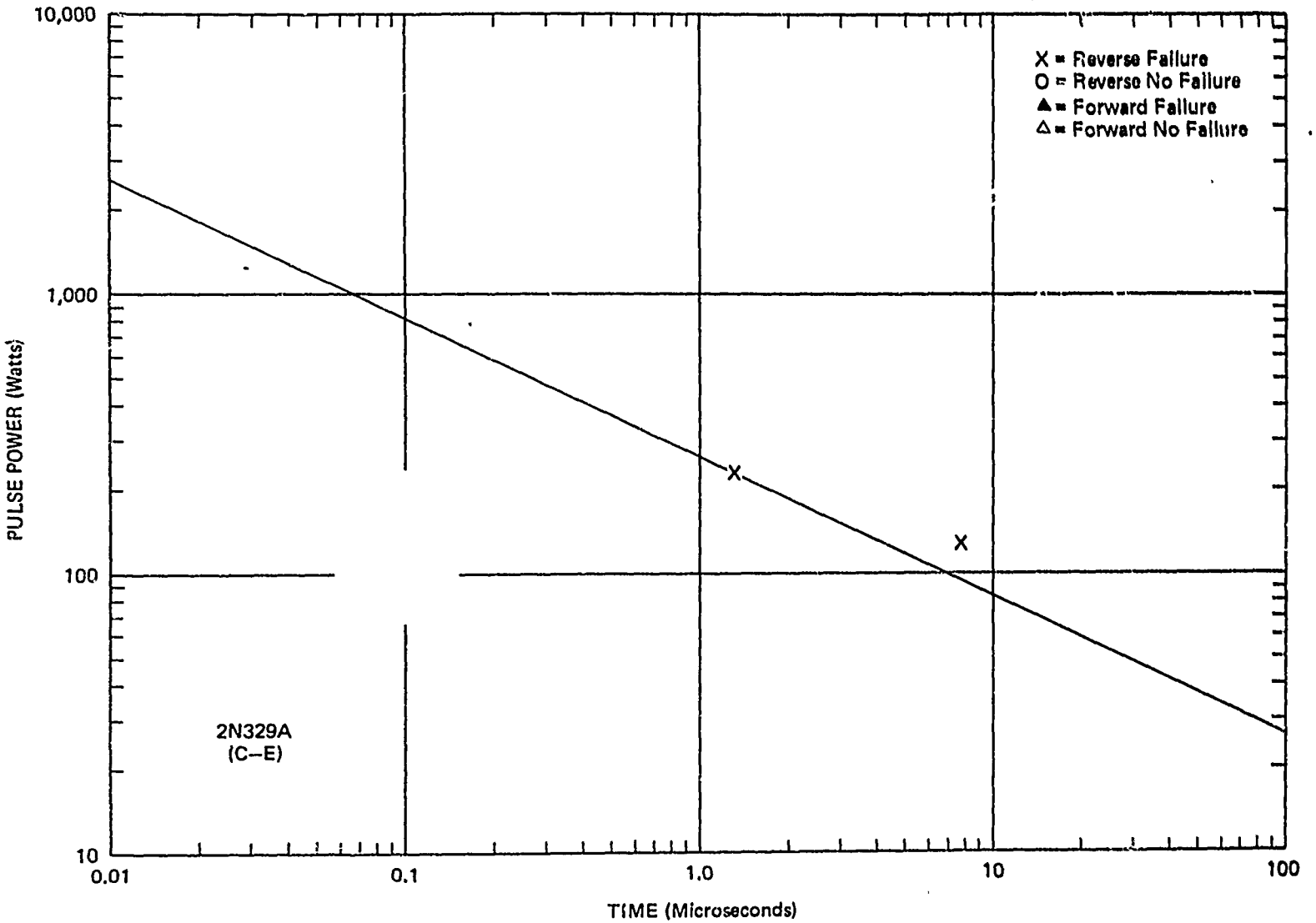

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2346
(C–A)
PULSE POWER (Watts)
10,000
1,000
100
10
TIME (Microseconds)
0.01
0.1
1.0
10
100

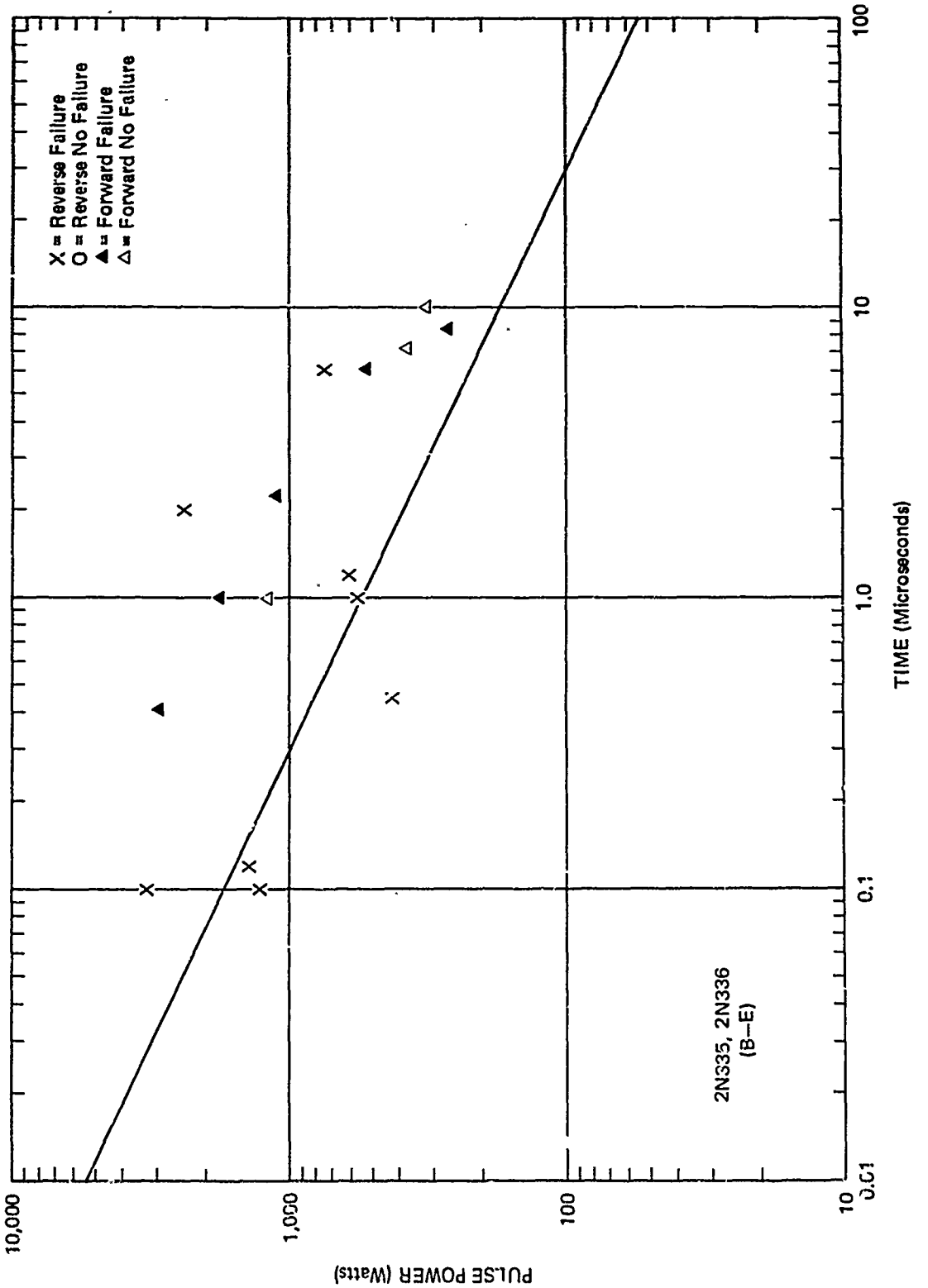

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2346
(C–G)

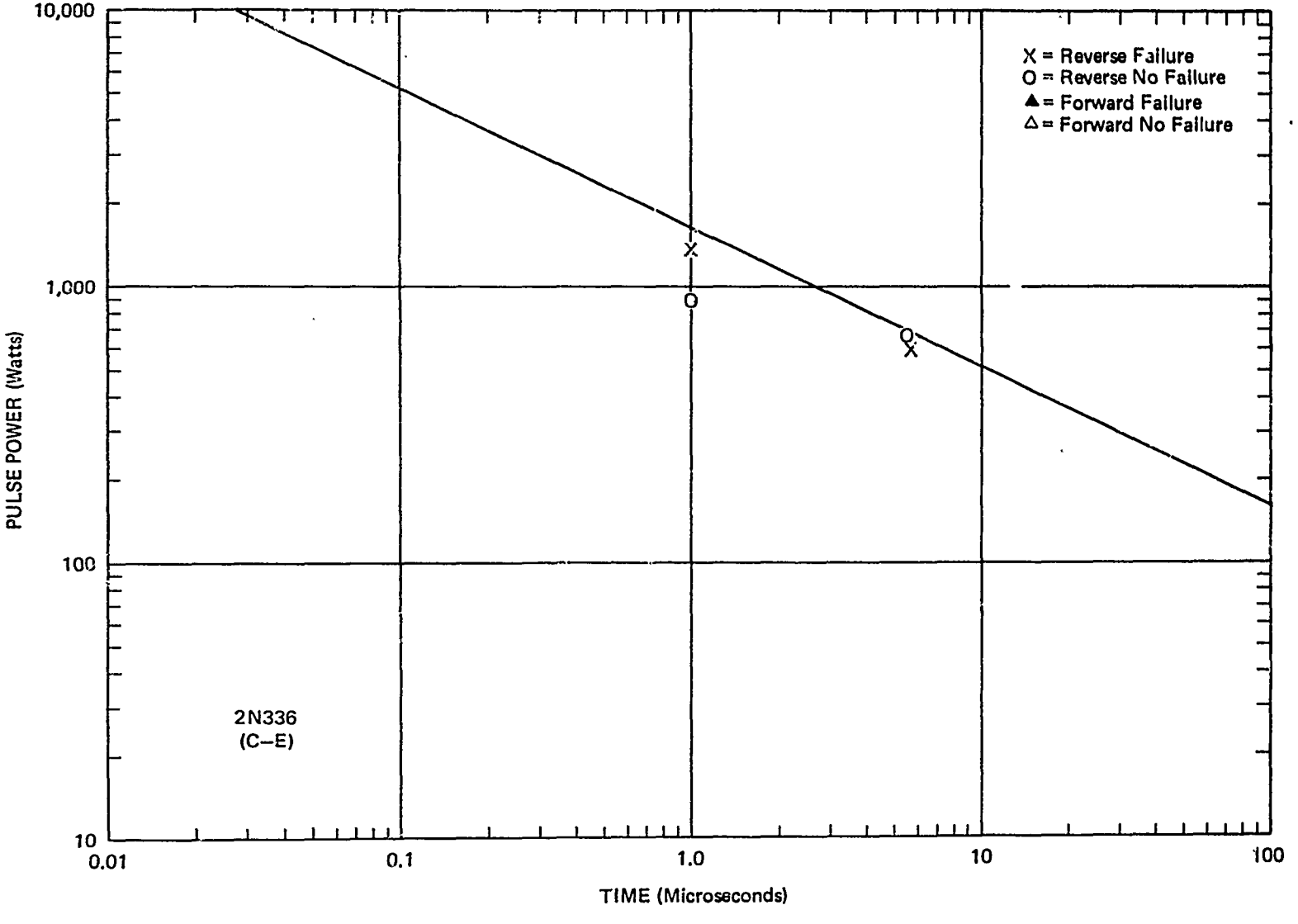
3.72

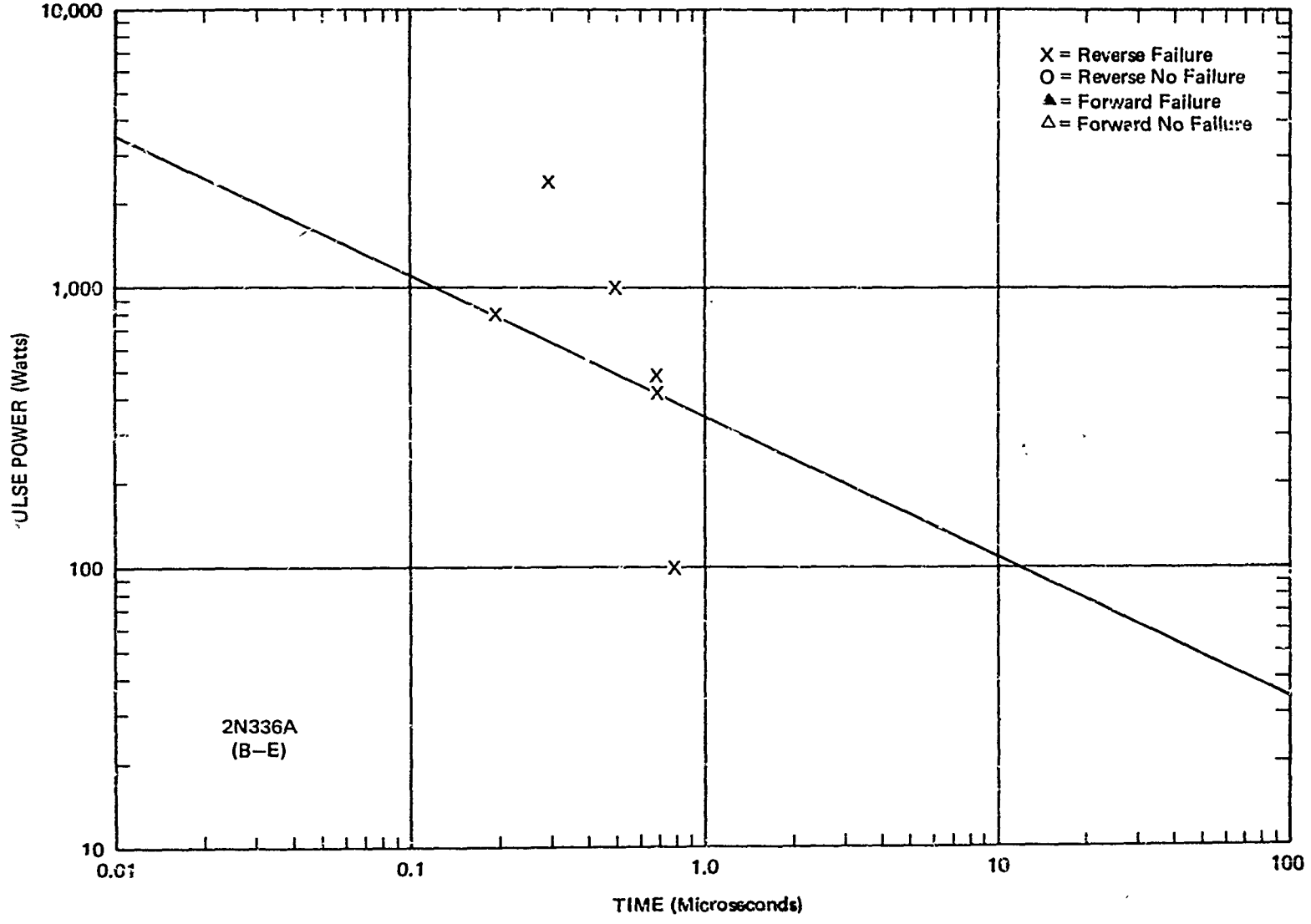

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17224/1-1
SCR TRANSITRON
C-G
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

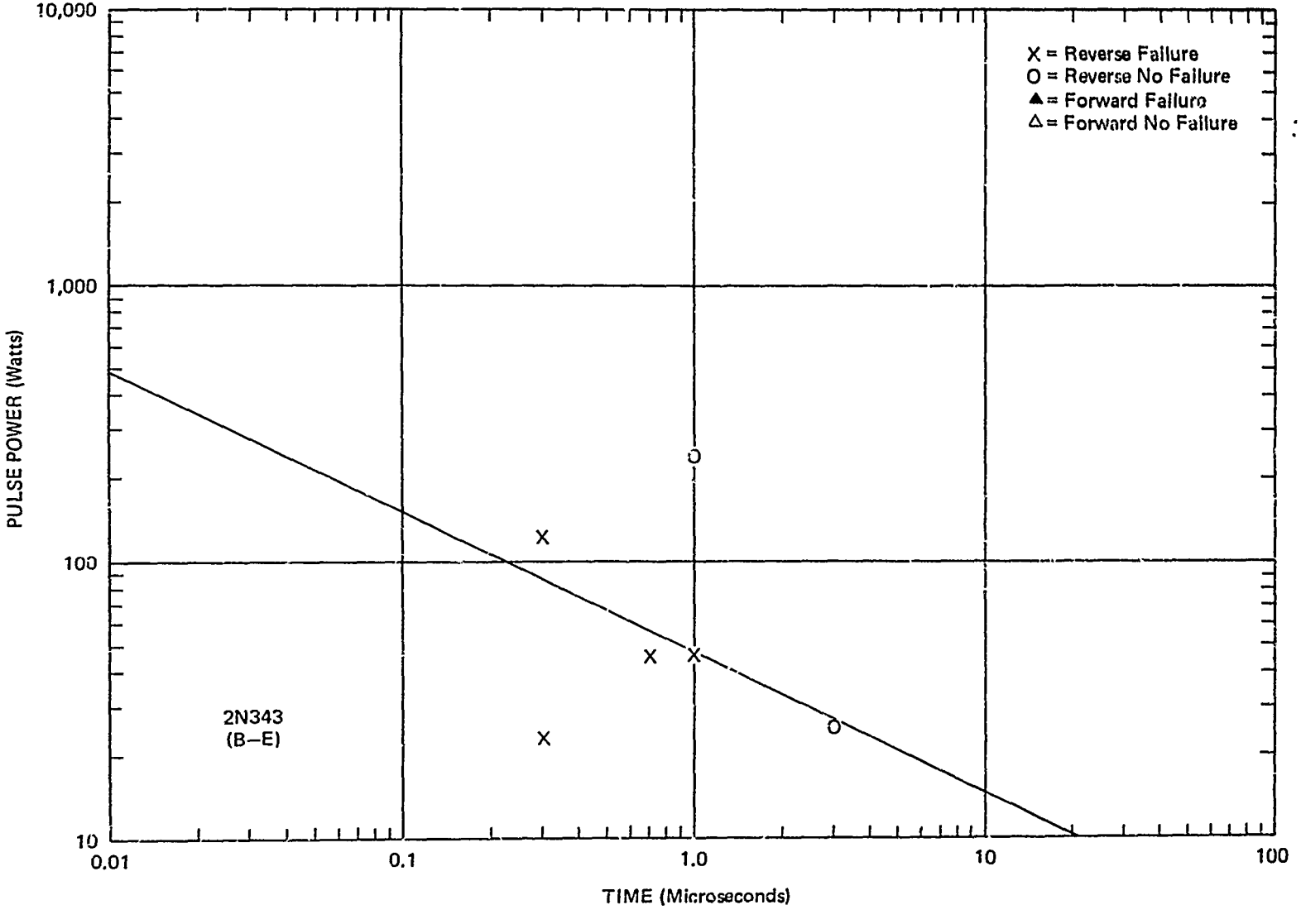

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N329A
(B–E)

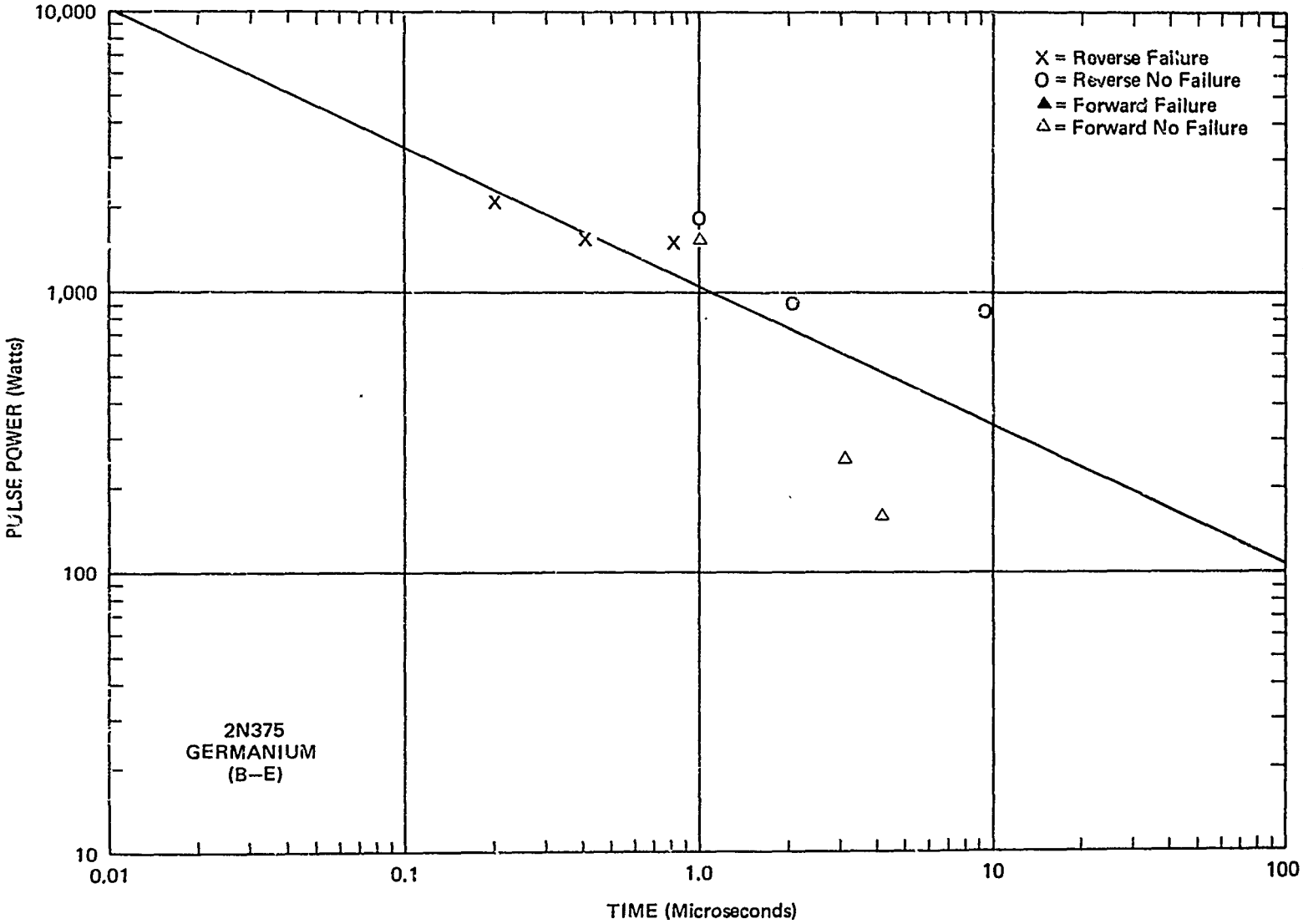

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N329A
(C–E)

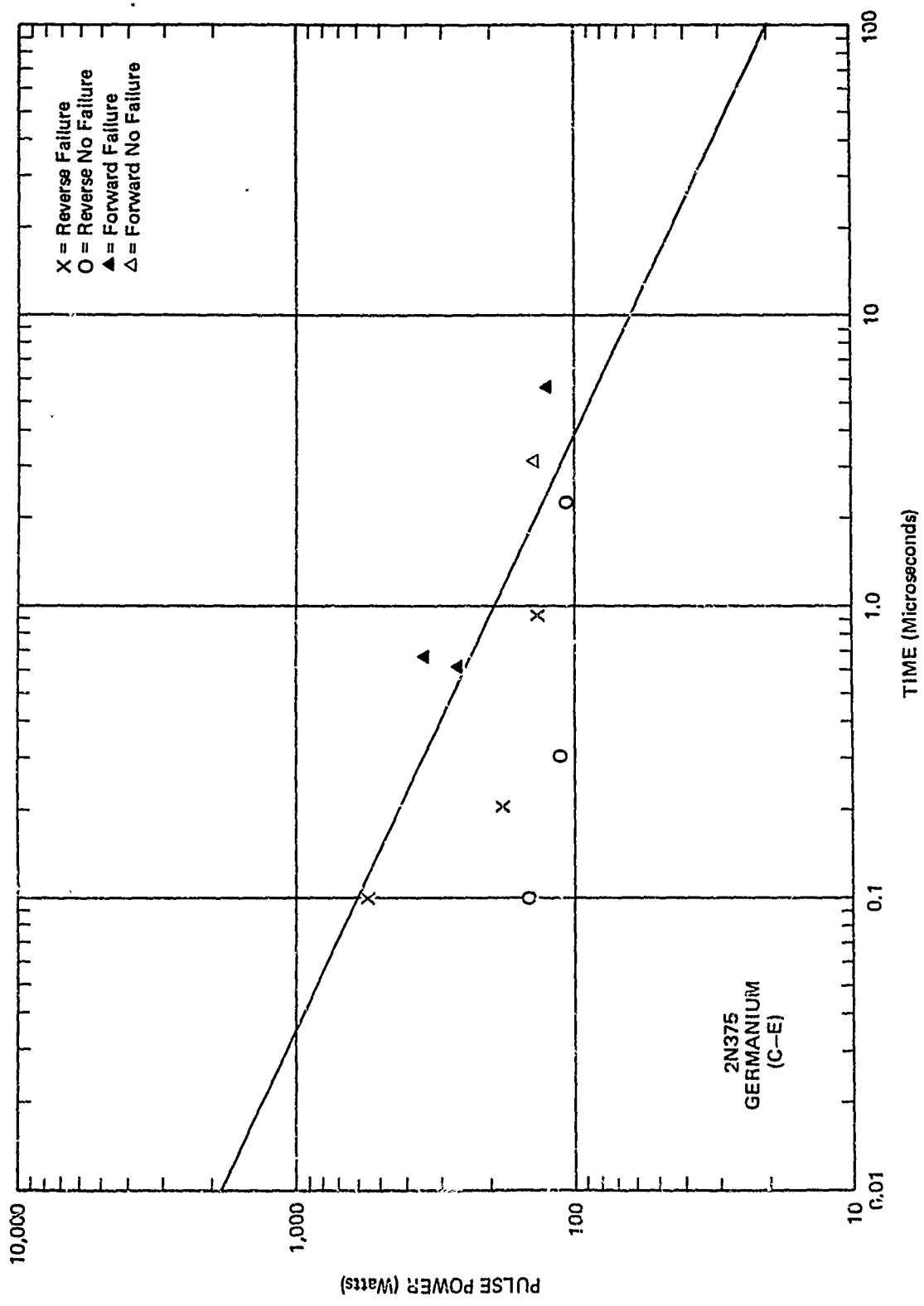

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N335, 2N336
(B–E)
PULSE POWER (Watts)
TIME (Microseconds)
10,000
1,000
100
10
0.01
0.1
1.0
10
100


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N336
(C–E)

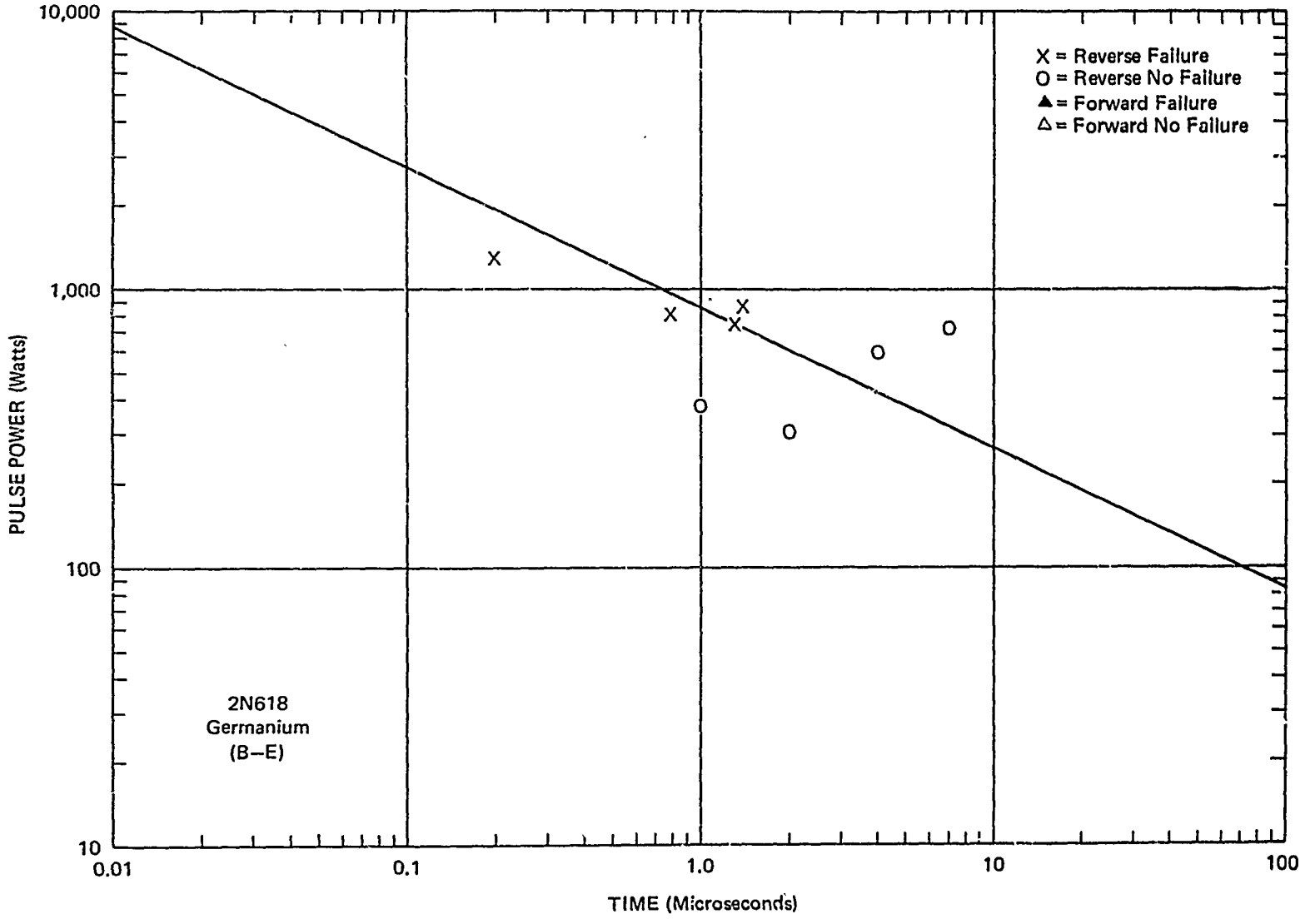

10,000
1,000
100
10
0.01
0.1
1.0
10
100
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N336A
(B–E)
PULSE POWER (Watts)
TIME (Microseconds)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N343
(B–E)

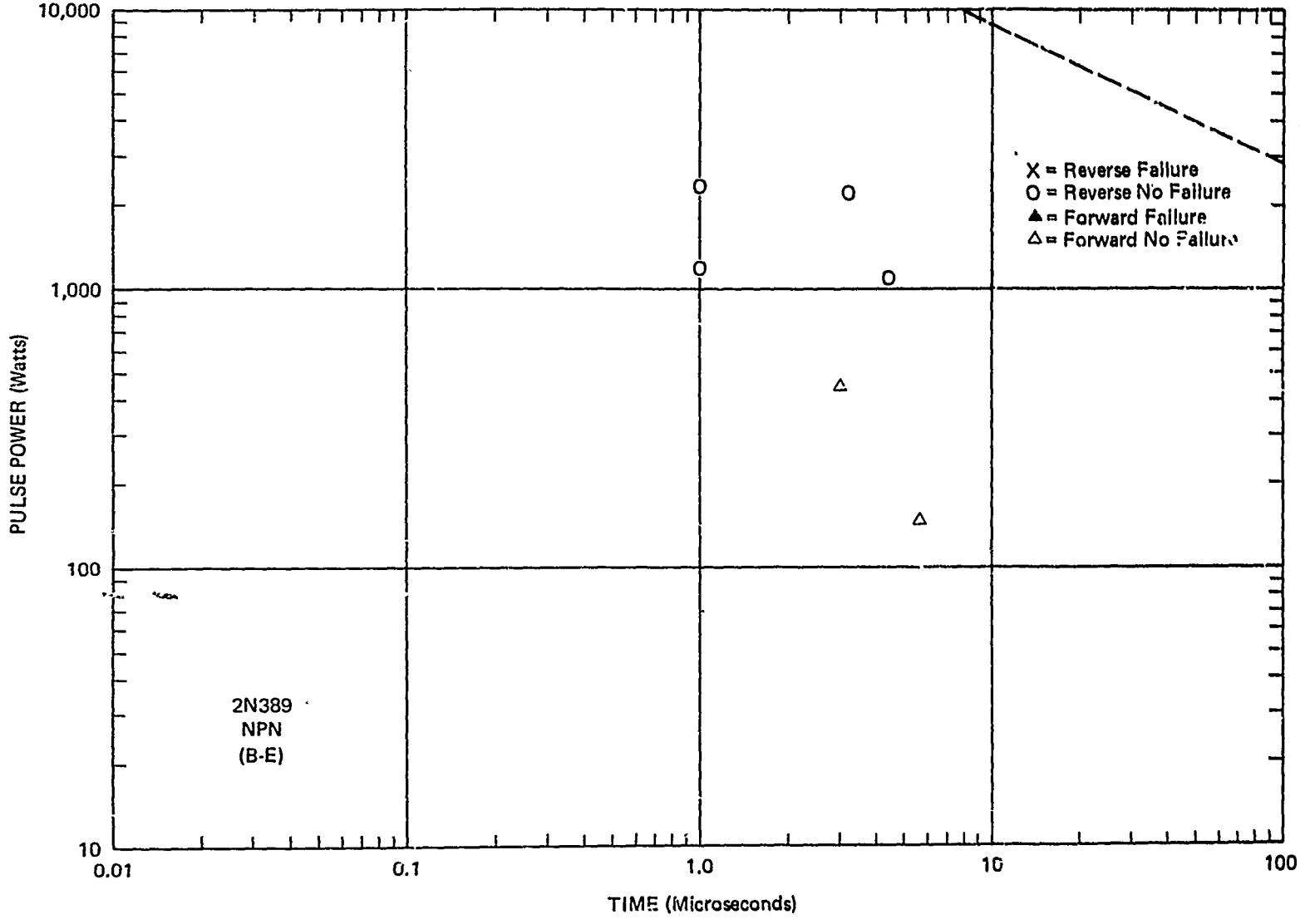

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N375
GERMANIUM
(B–E)


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N375
GERMANIUM
(C–E)
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

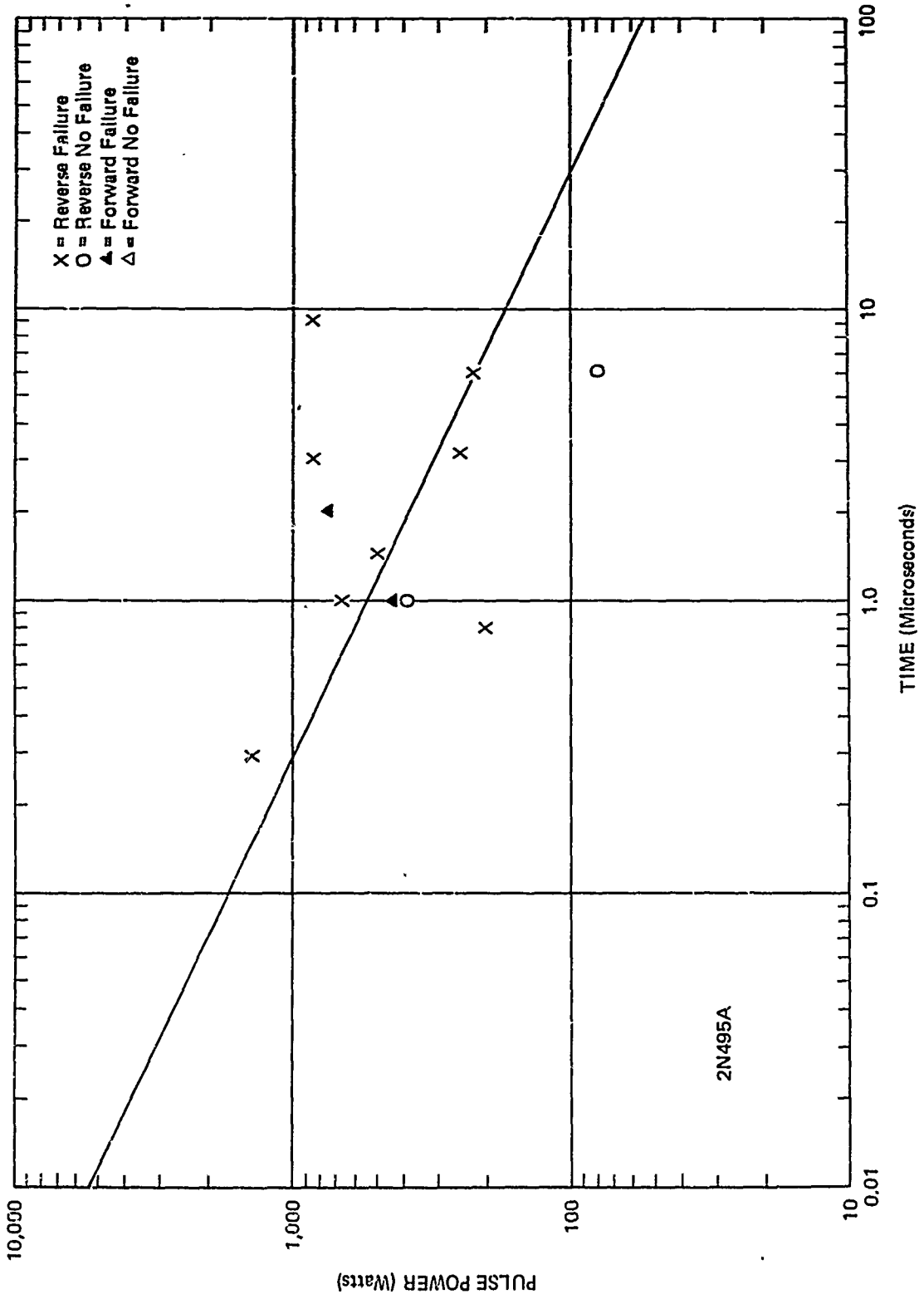
3.81


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N618
Germanium
(B–E)

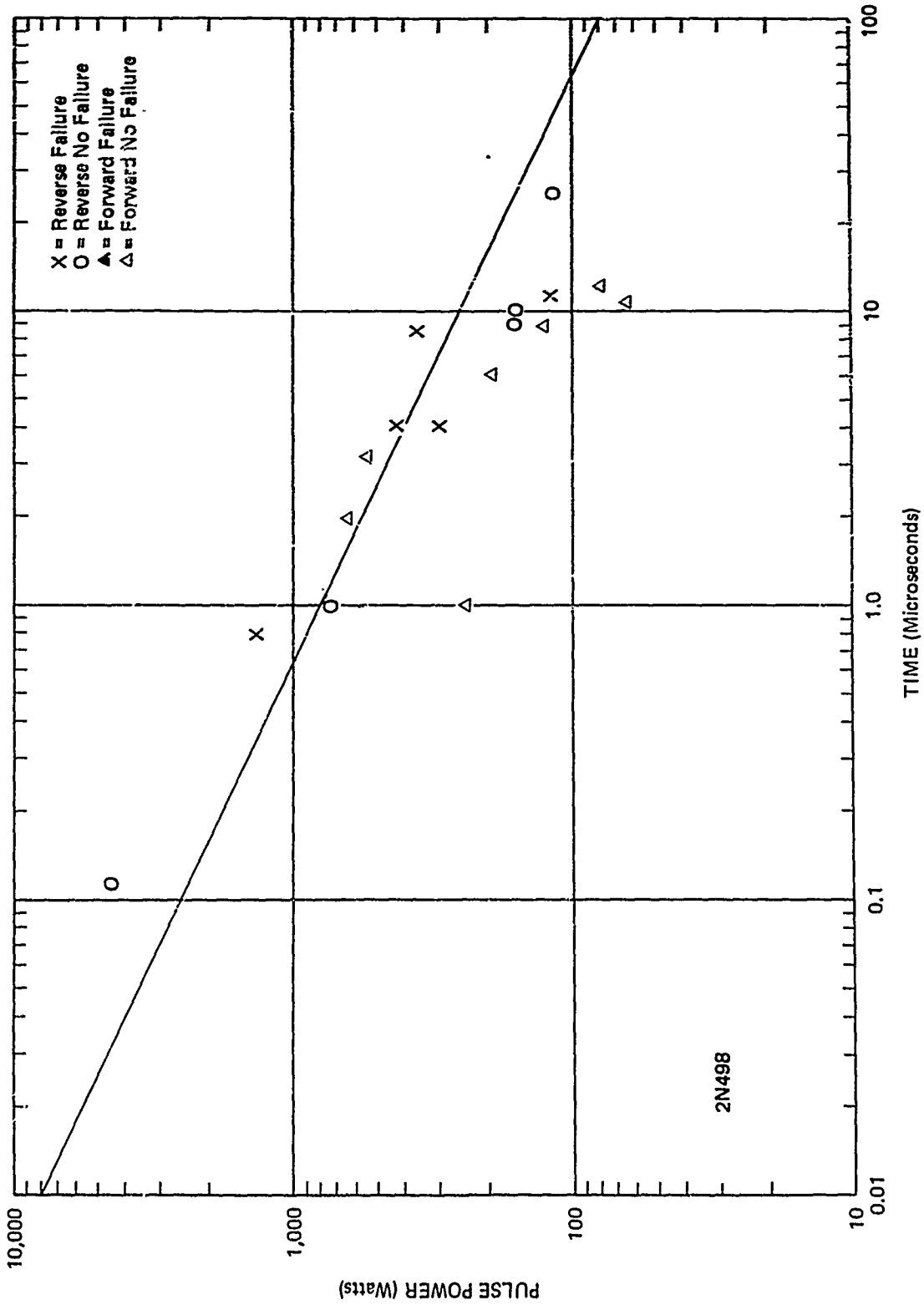
3-82


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N389
NPN
(B-E)

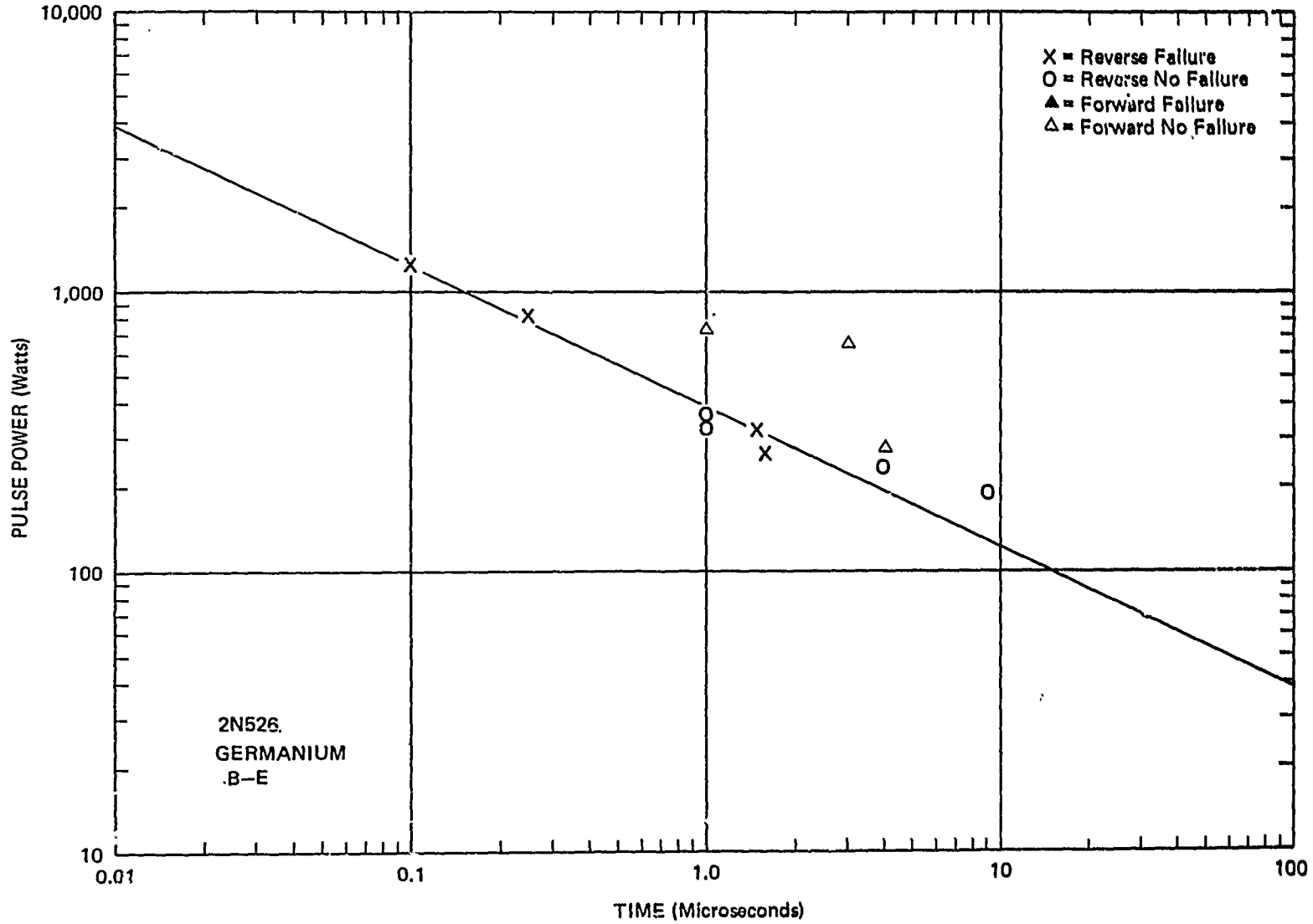
3.83


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N495A
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

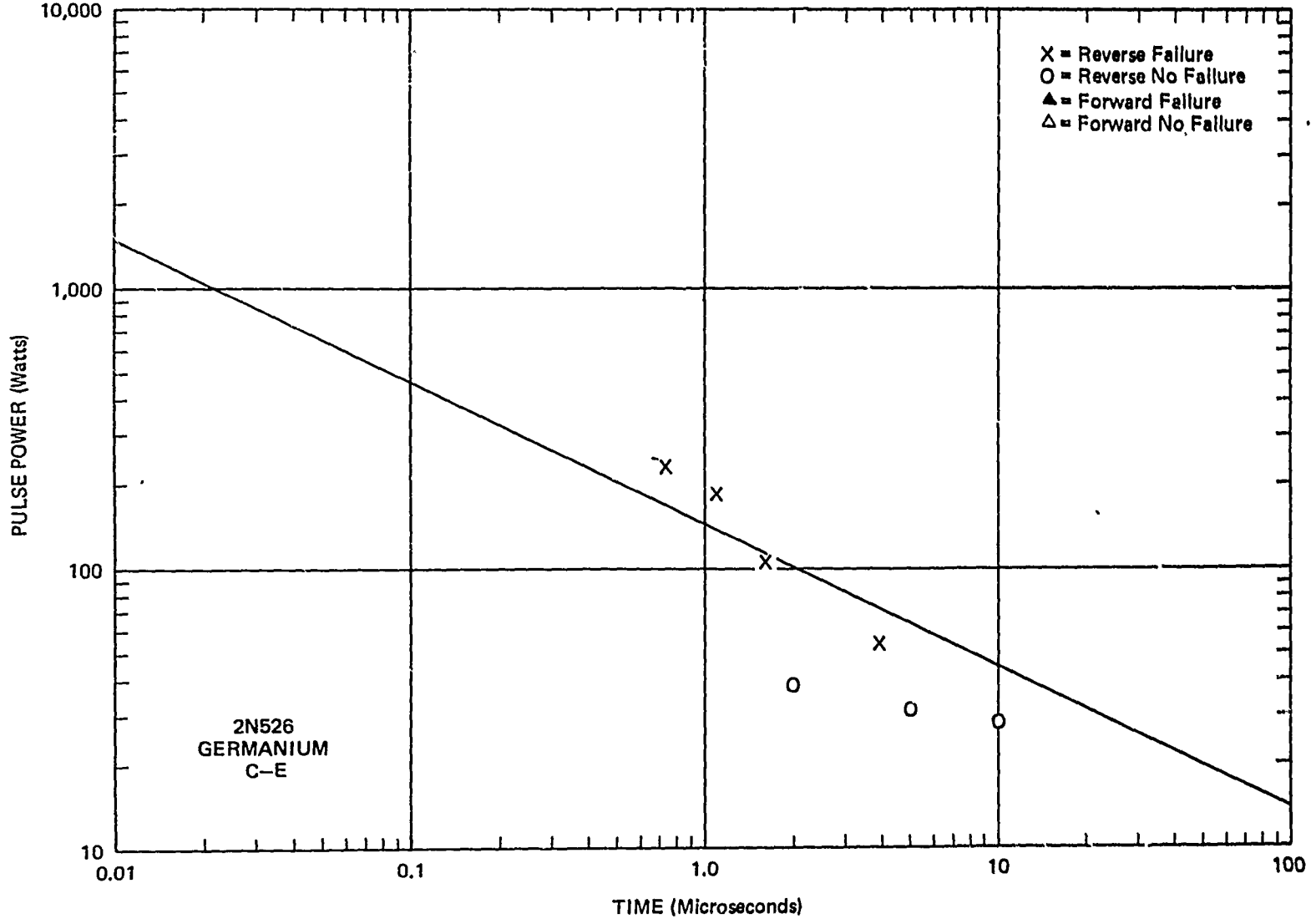
3.84


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N498
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

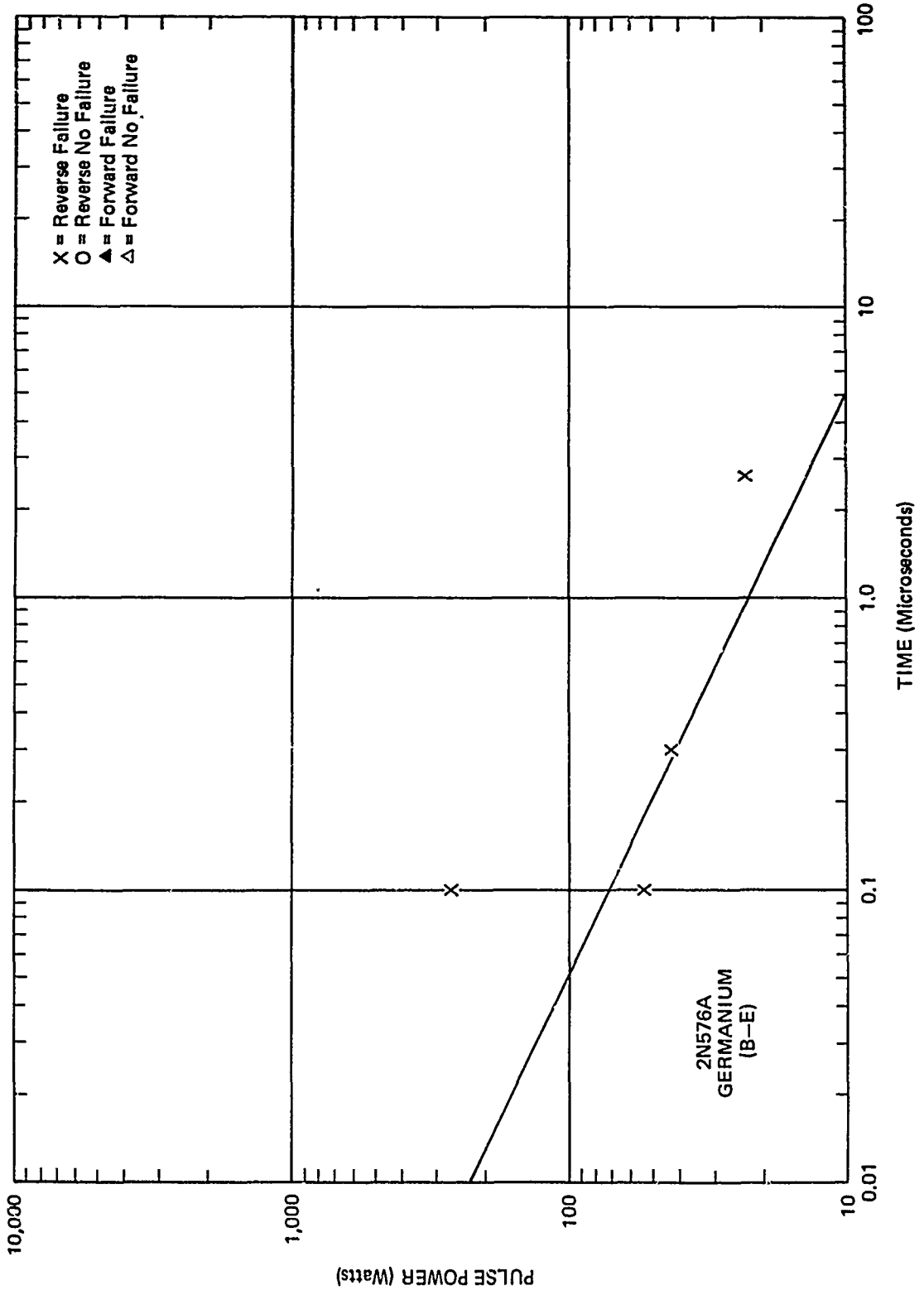
3.85


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N526
GERMANIUM
B–E

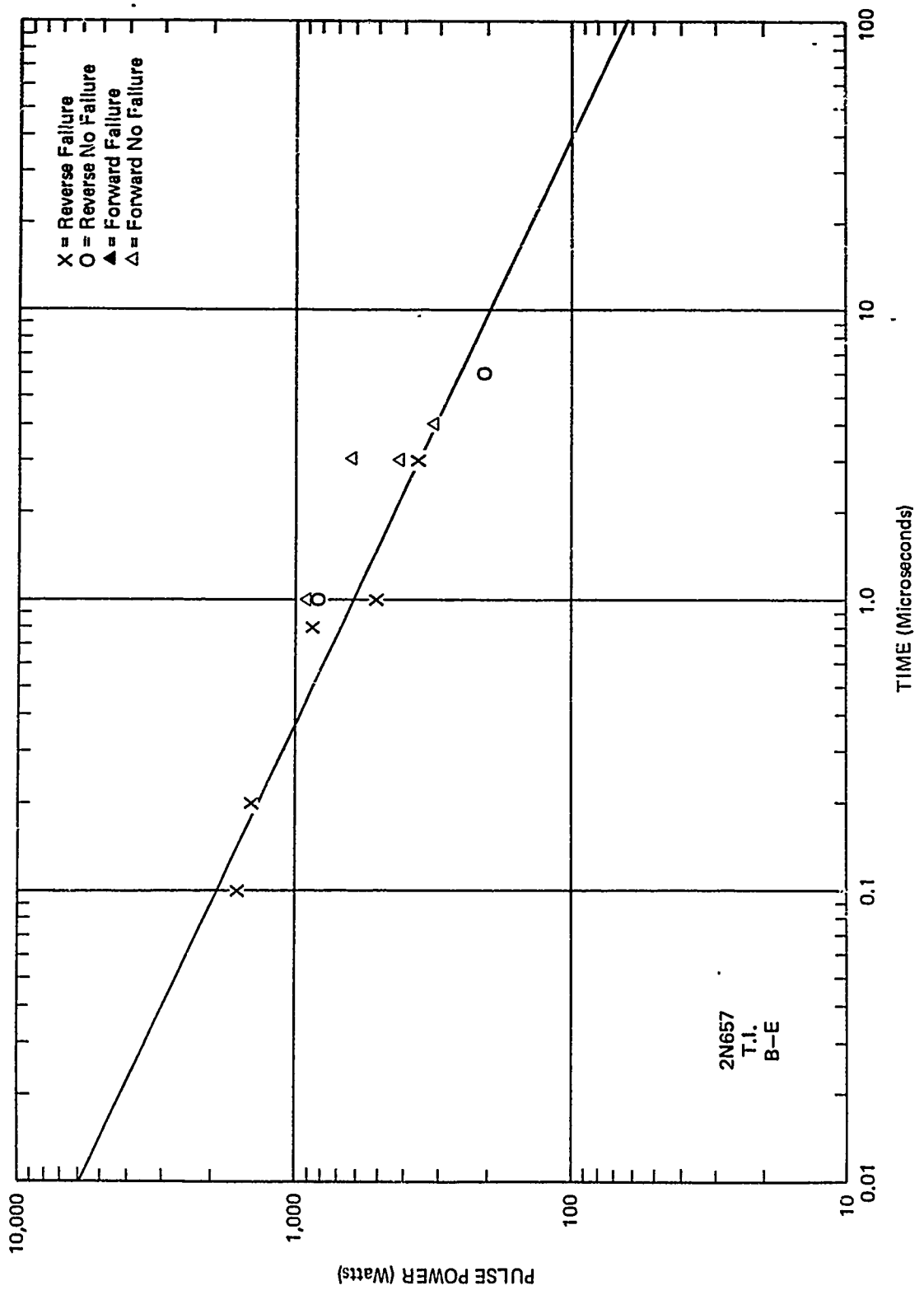
3.86


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N526
GERMANIUM
C–E

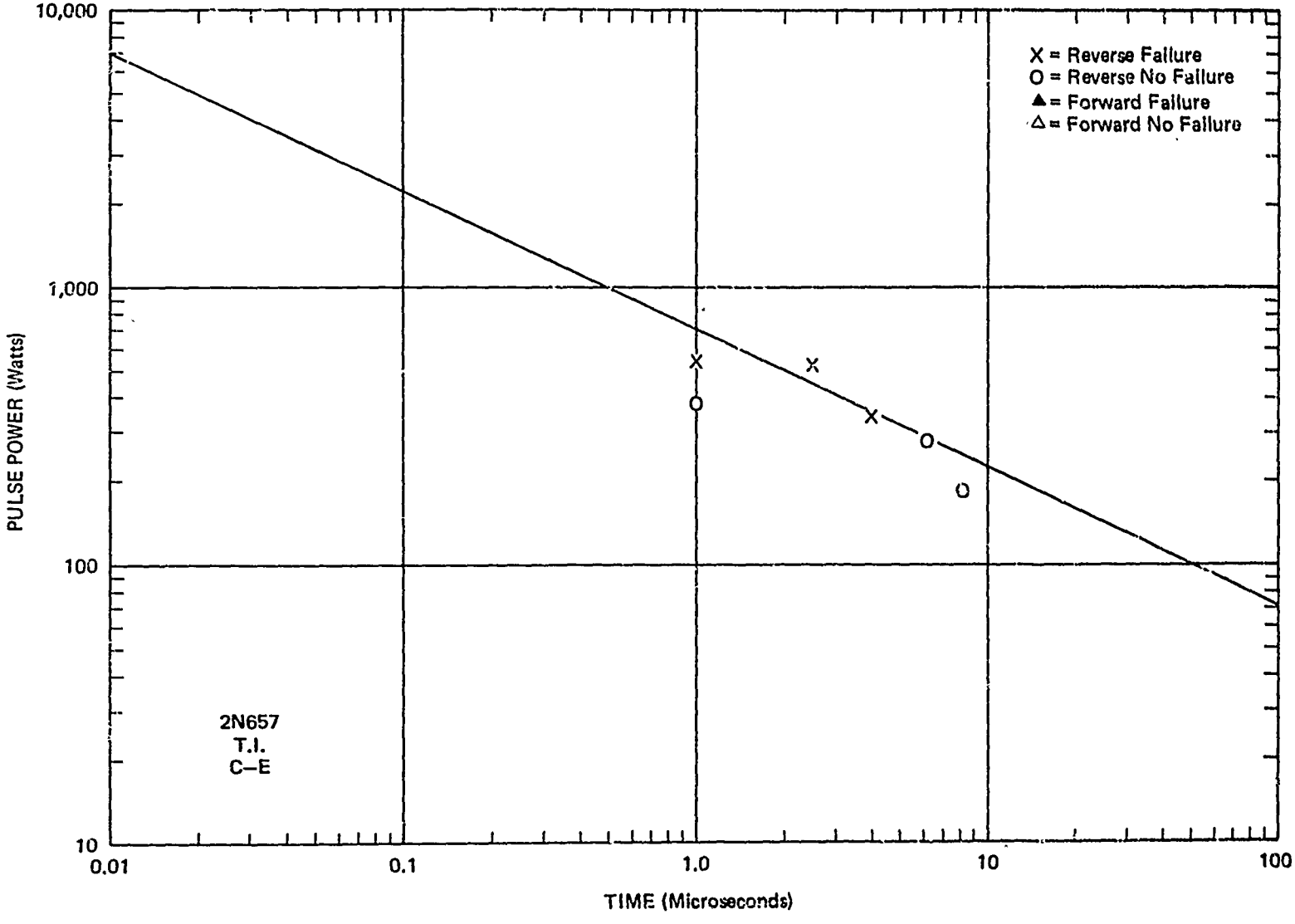
3.87


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N576A
GERMANIUM
(B–E)
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

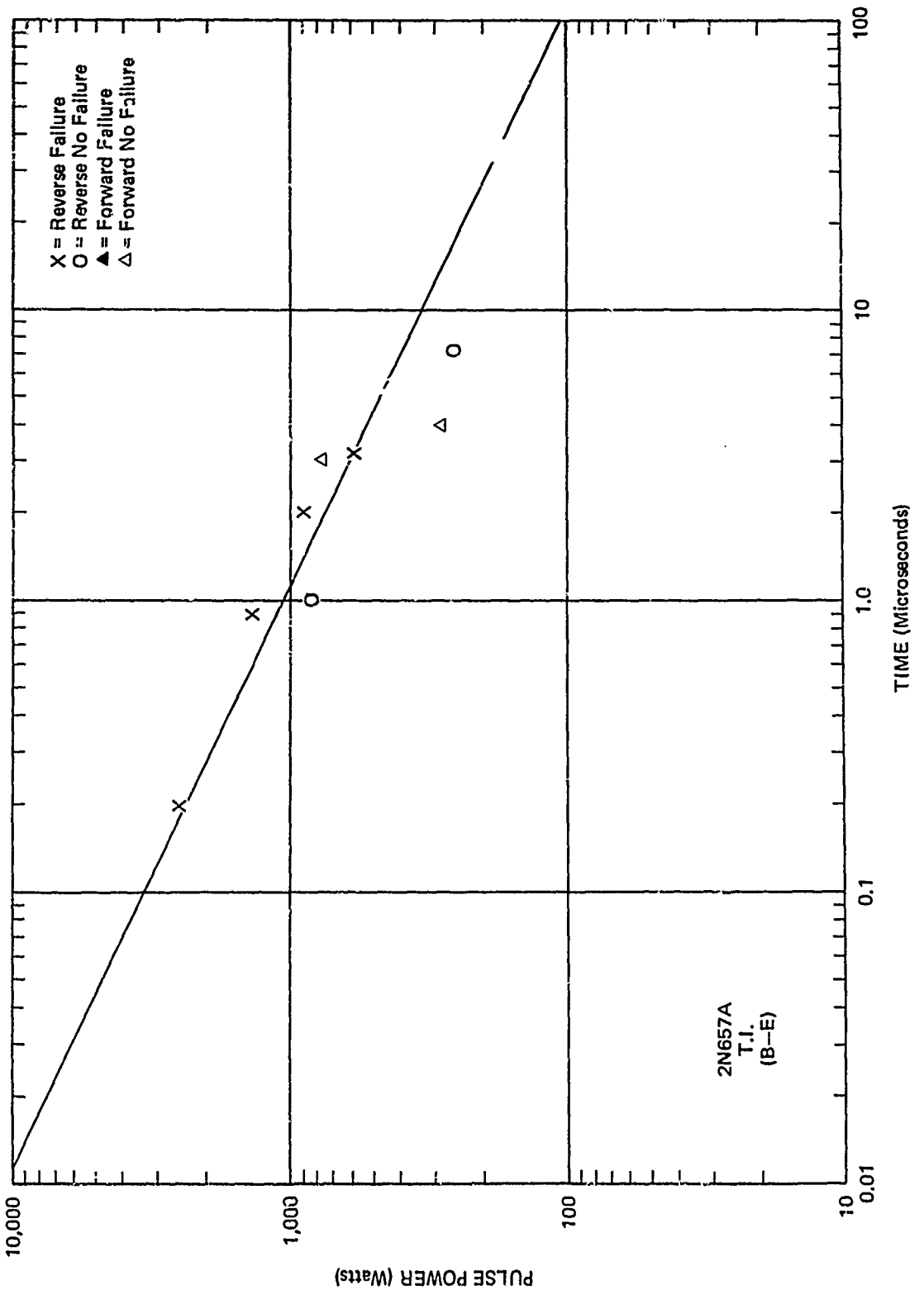
3.88

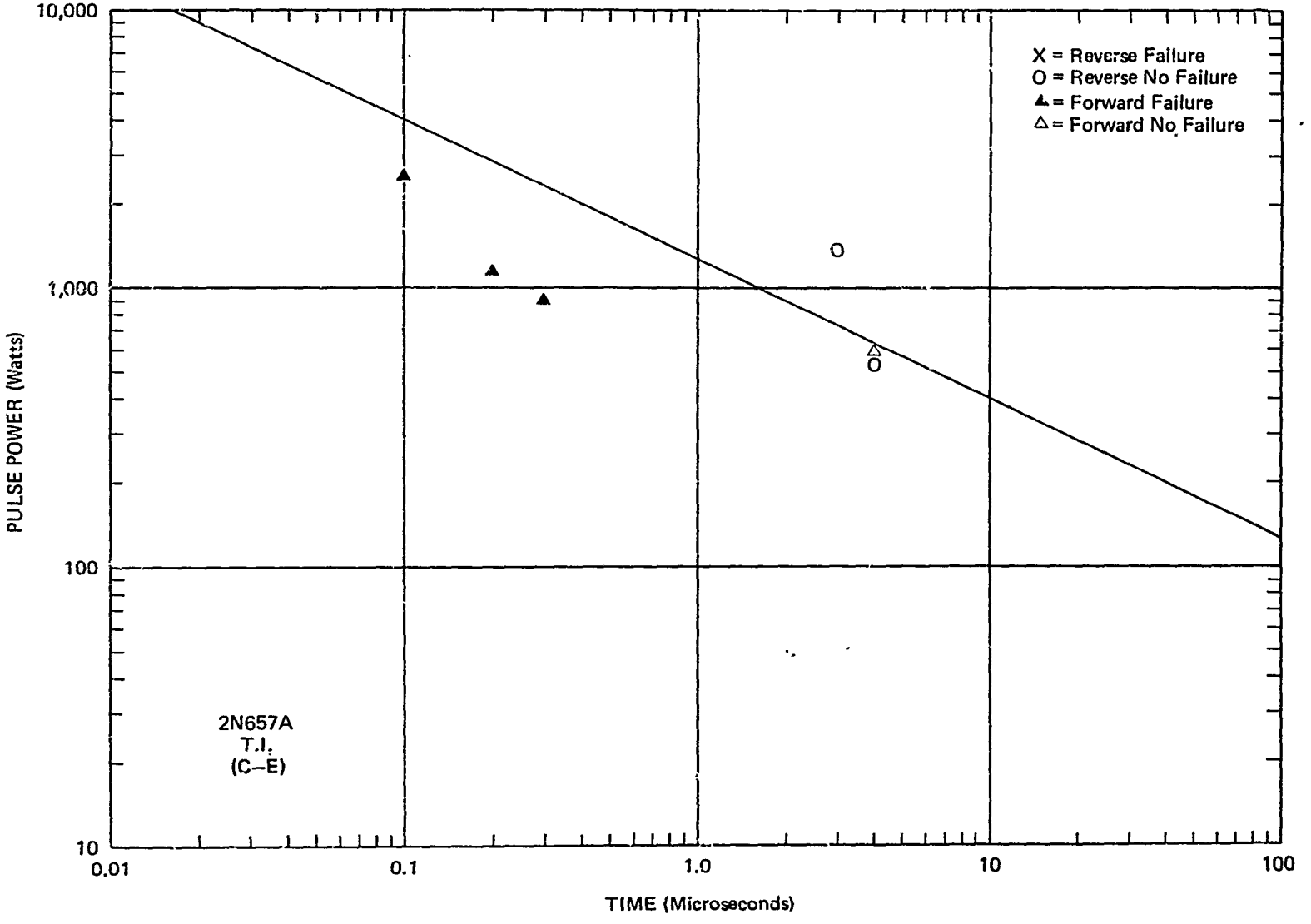

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657
T.I.
B-E
PULSE POWER (Watts)
10,000
1,000
100
10
TIME (Microseconds)
0.01
0.1
1.0
10
100

3.89

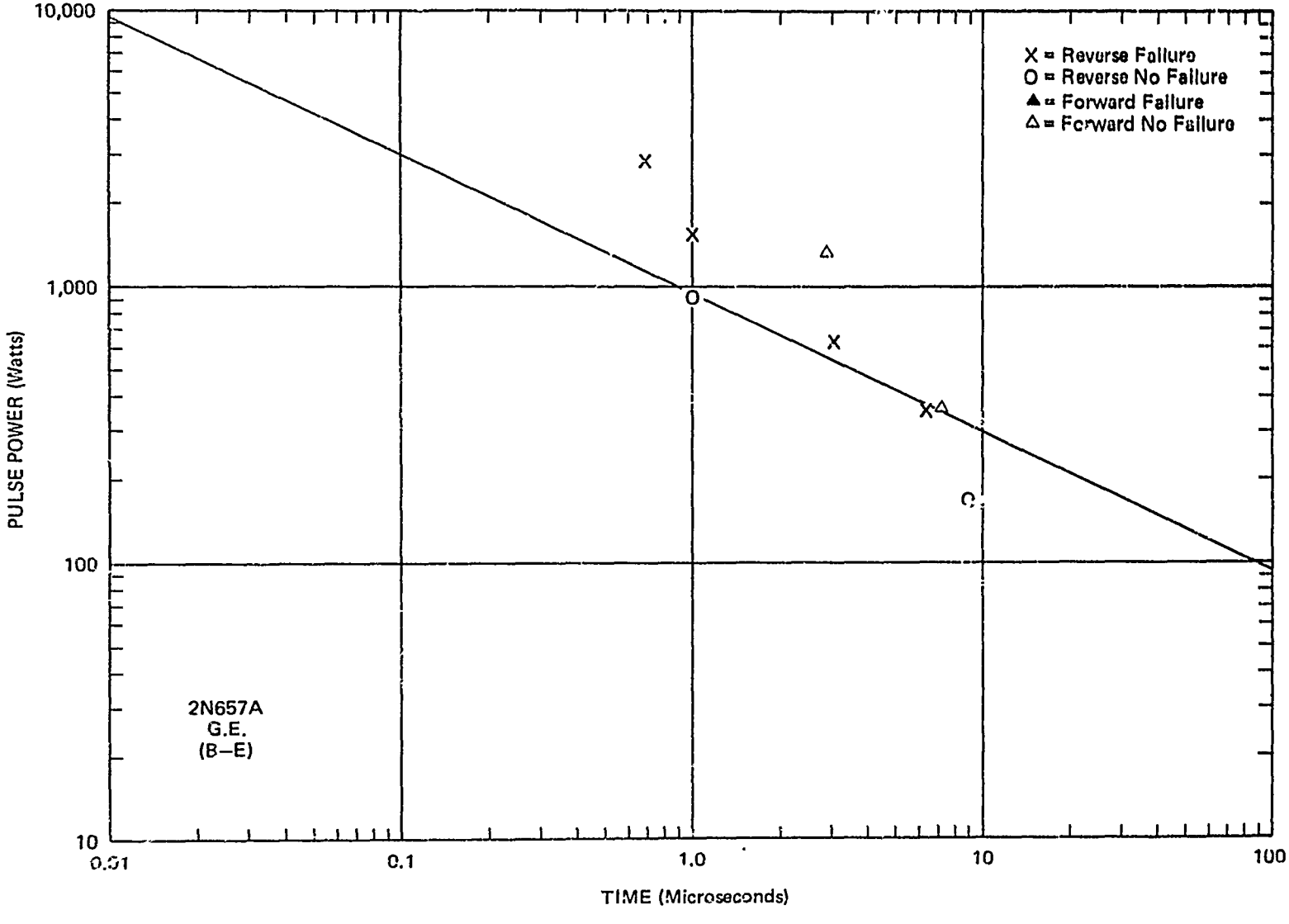

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657
T.I.
C–E

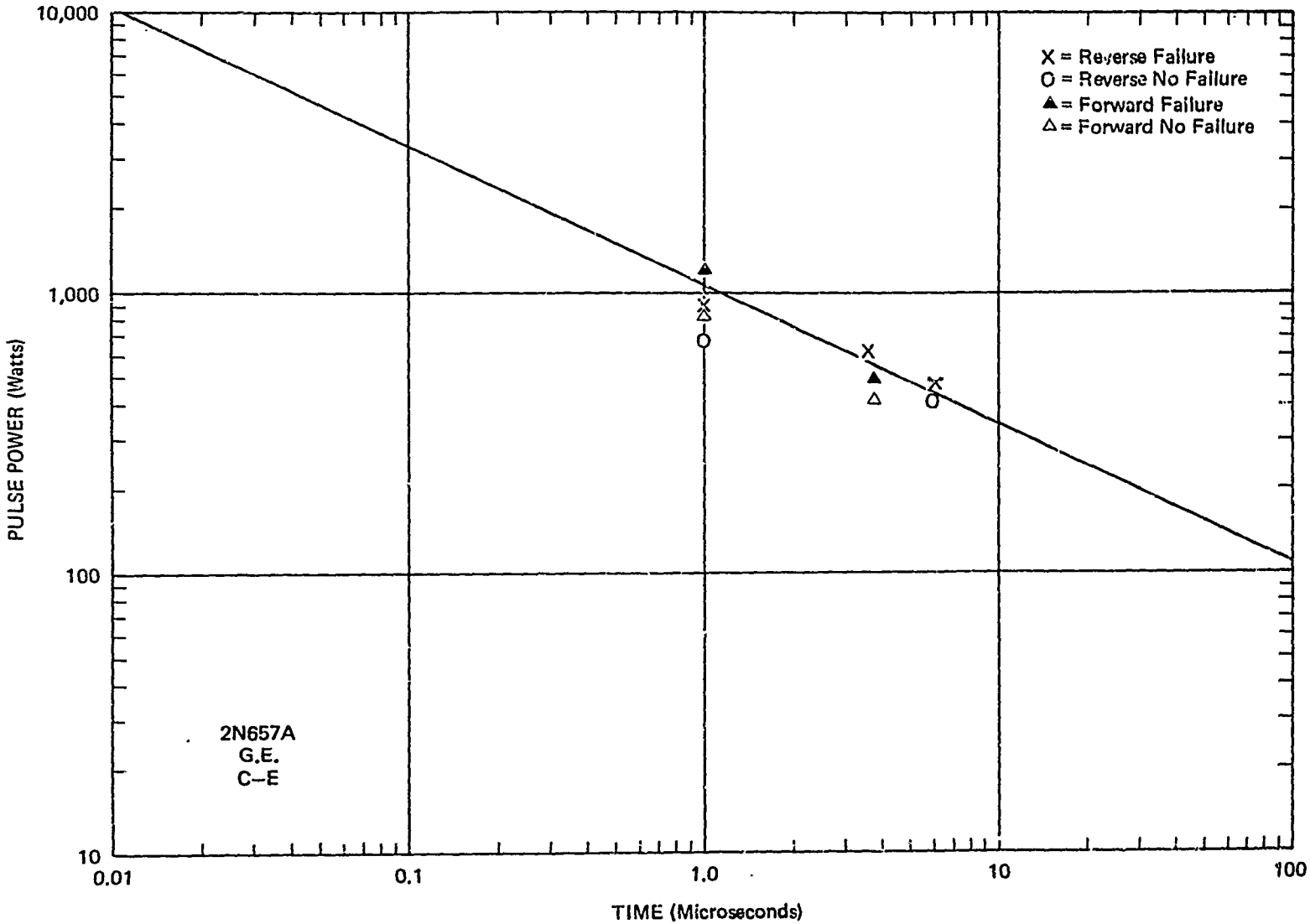
3.90


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657A
T.I.
(B—E)
PULSE POWER (Watts)
10,000
1,000
100
10
TIME (Microseconds)
0.01
0.1
1.0
10
100


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657A
T.I.
(C–E)

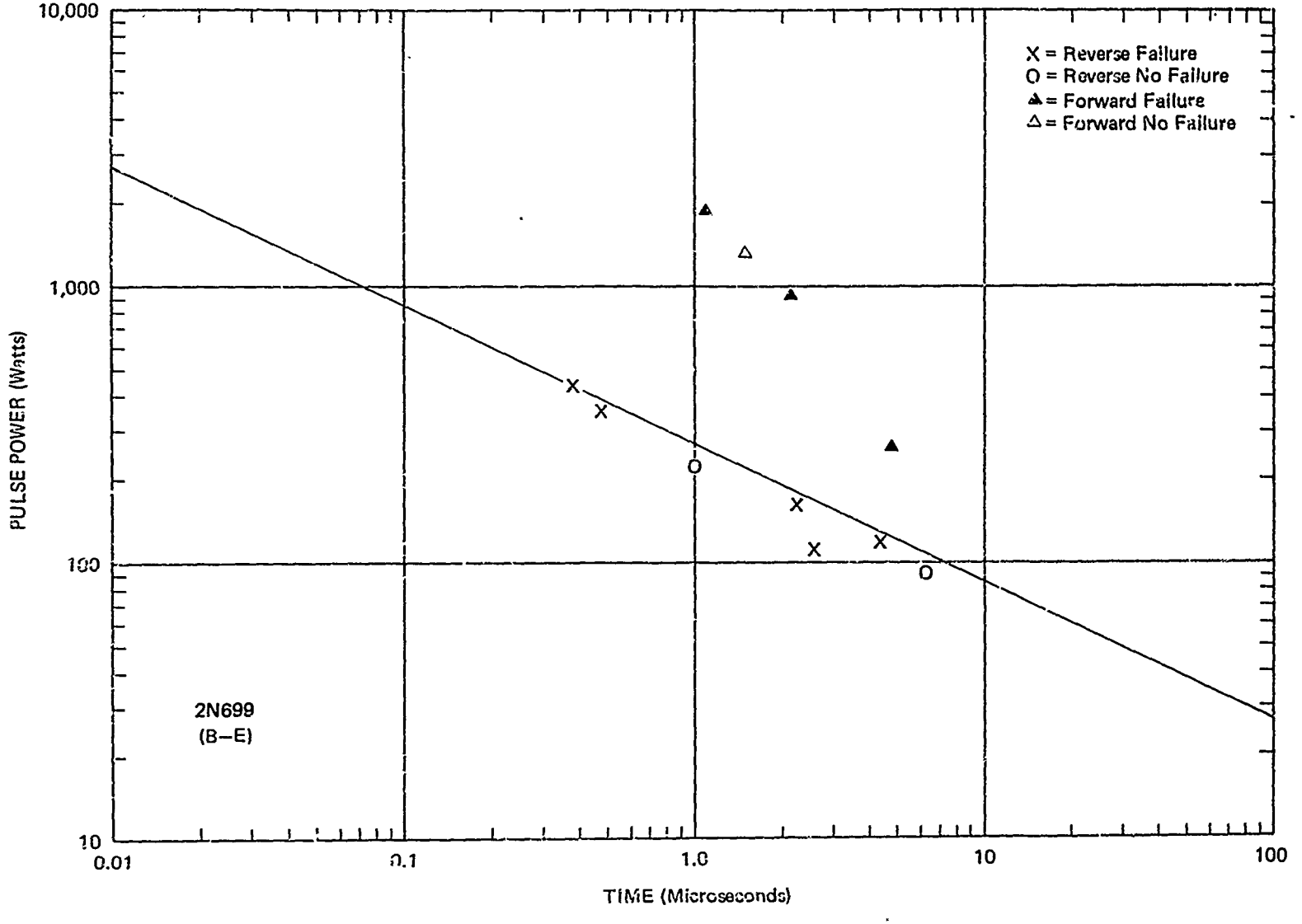
3.92


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657A
G.E.
(B–E)


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N657A
G.E.
C–E

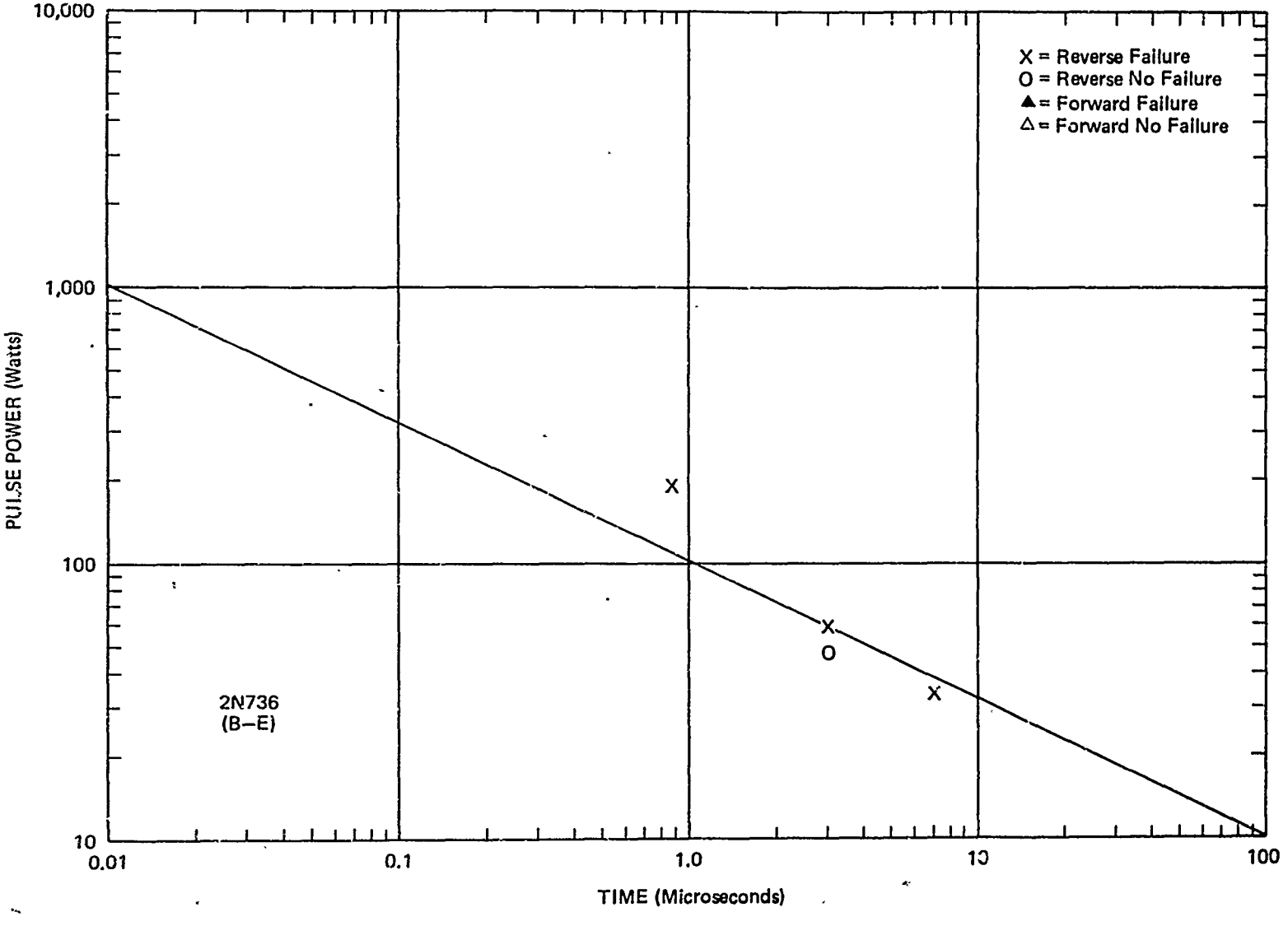
3.94

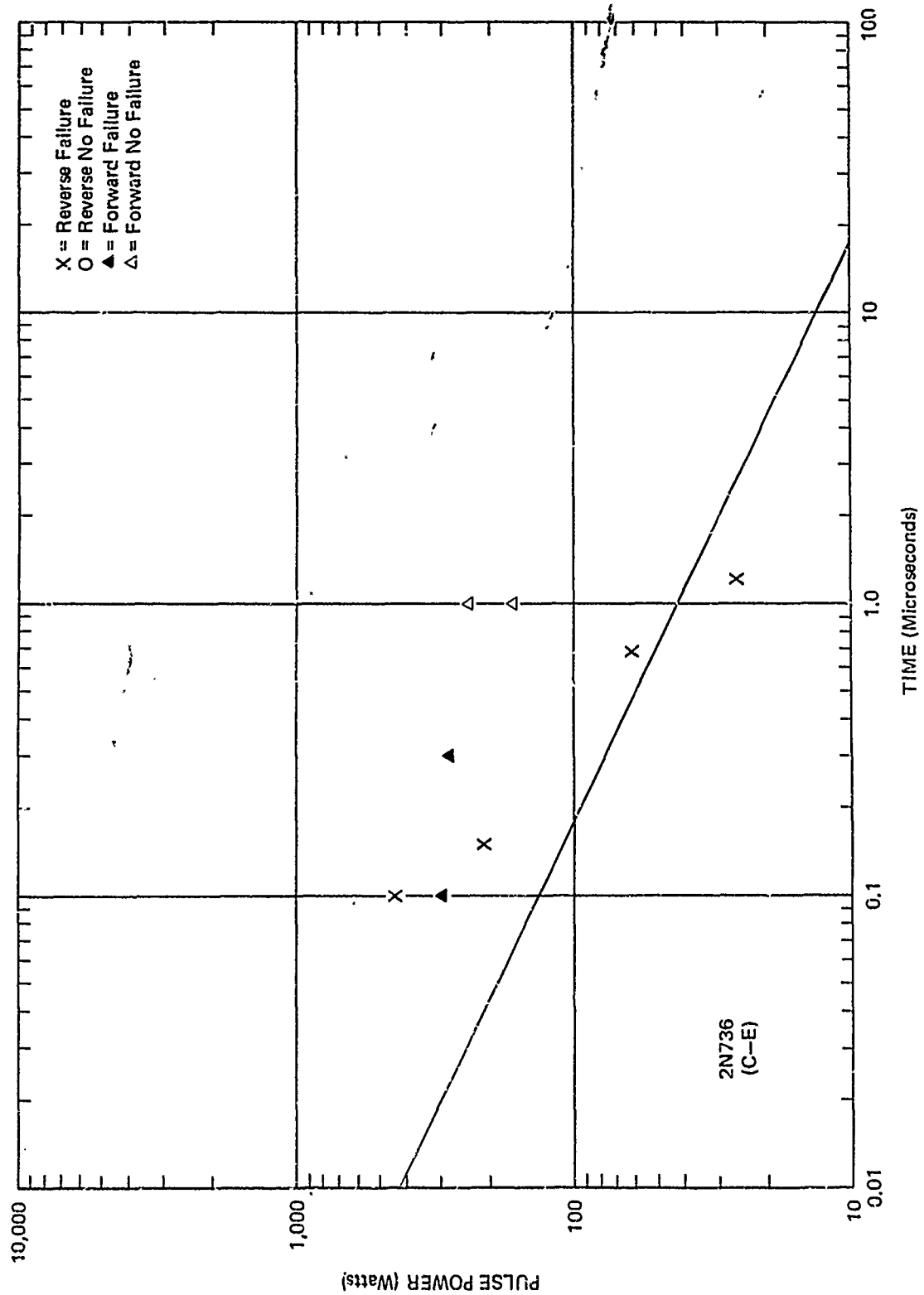
148


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N699
(B–E)

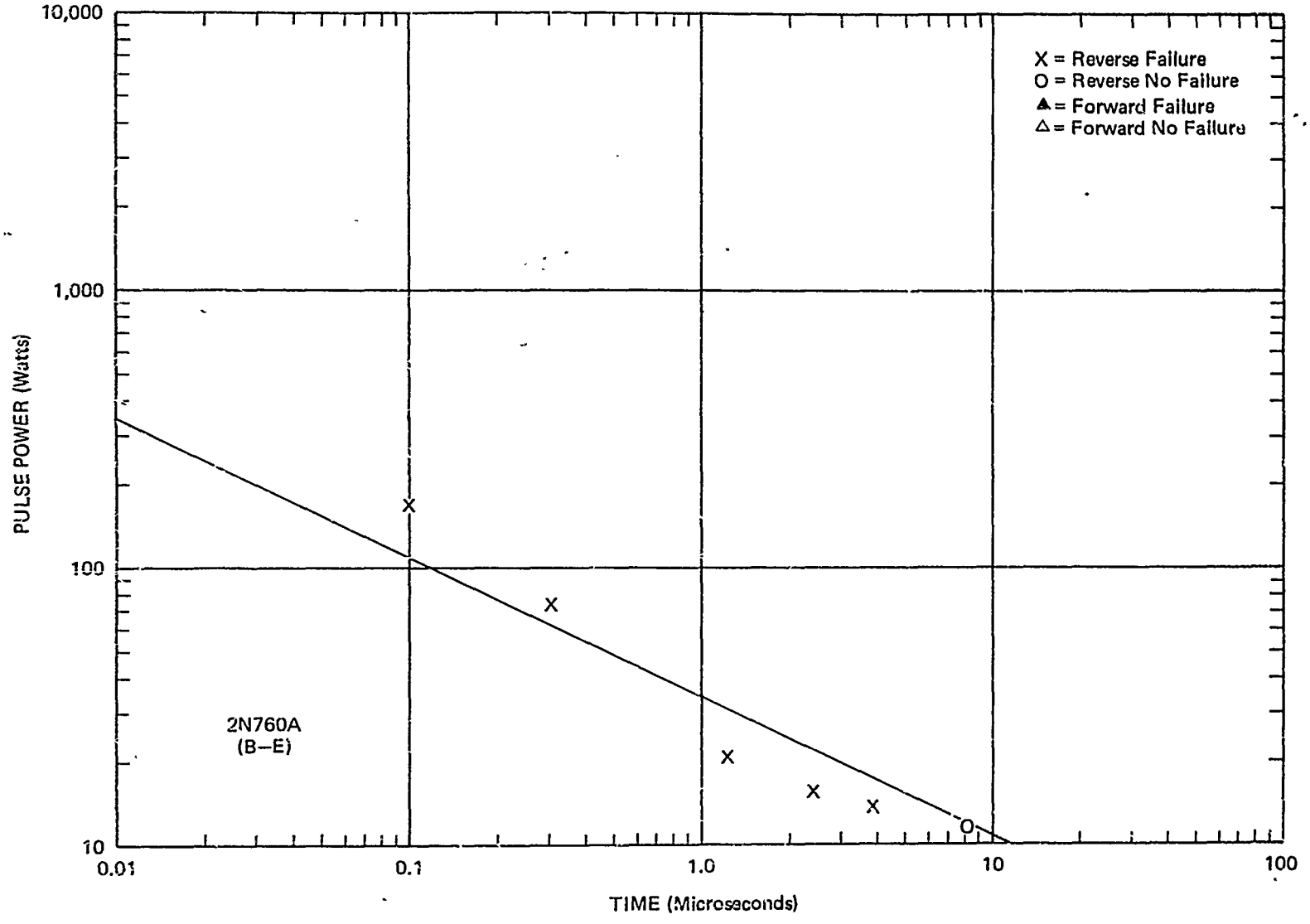
3.95

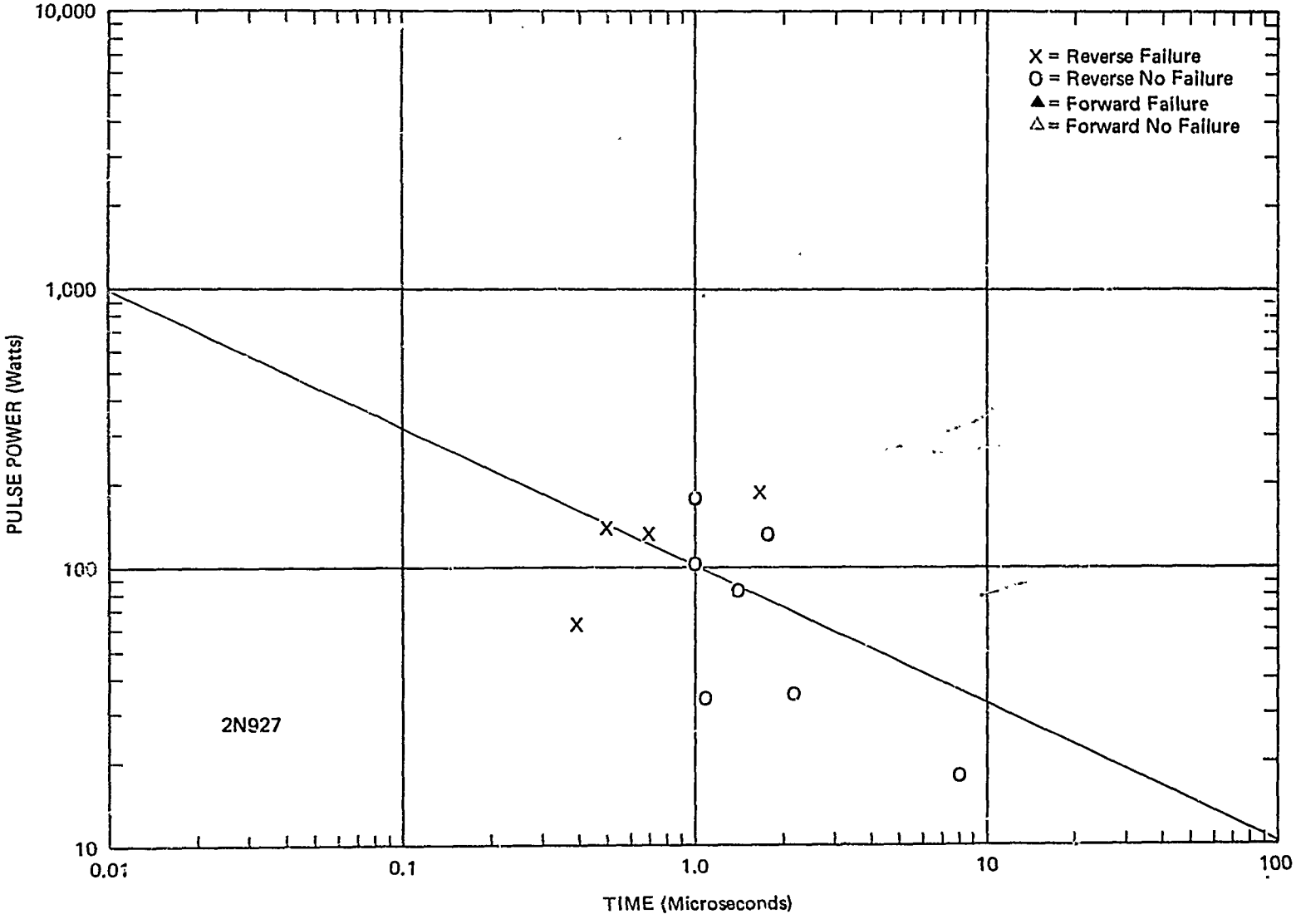
T-93


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N736
(B–E)

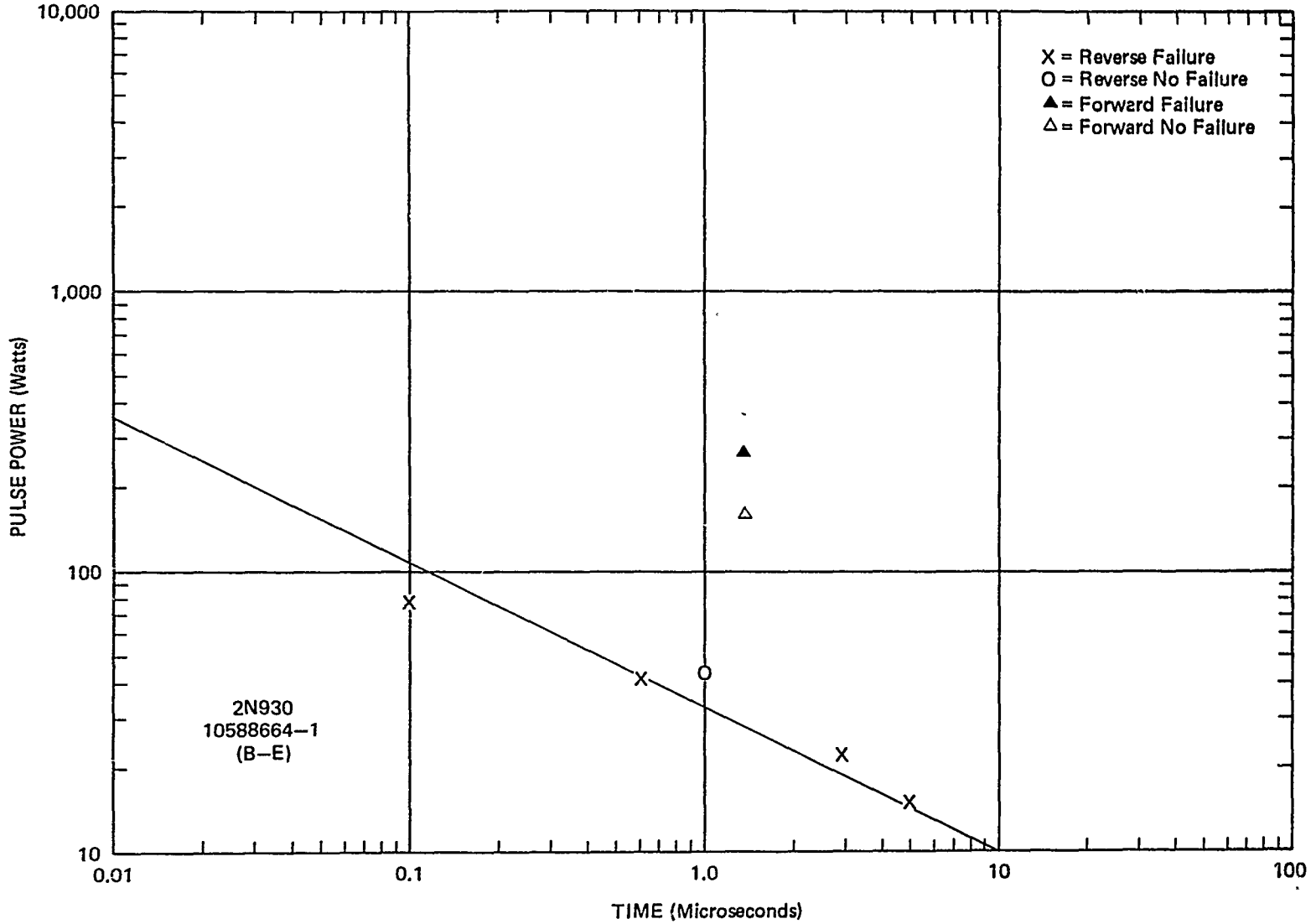

X = Reverse Failure
O = Reverse No Failure
◀ = Forward Failure
△ = Forward No Failure
2N736
(C–E)
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.97

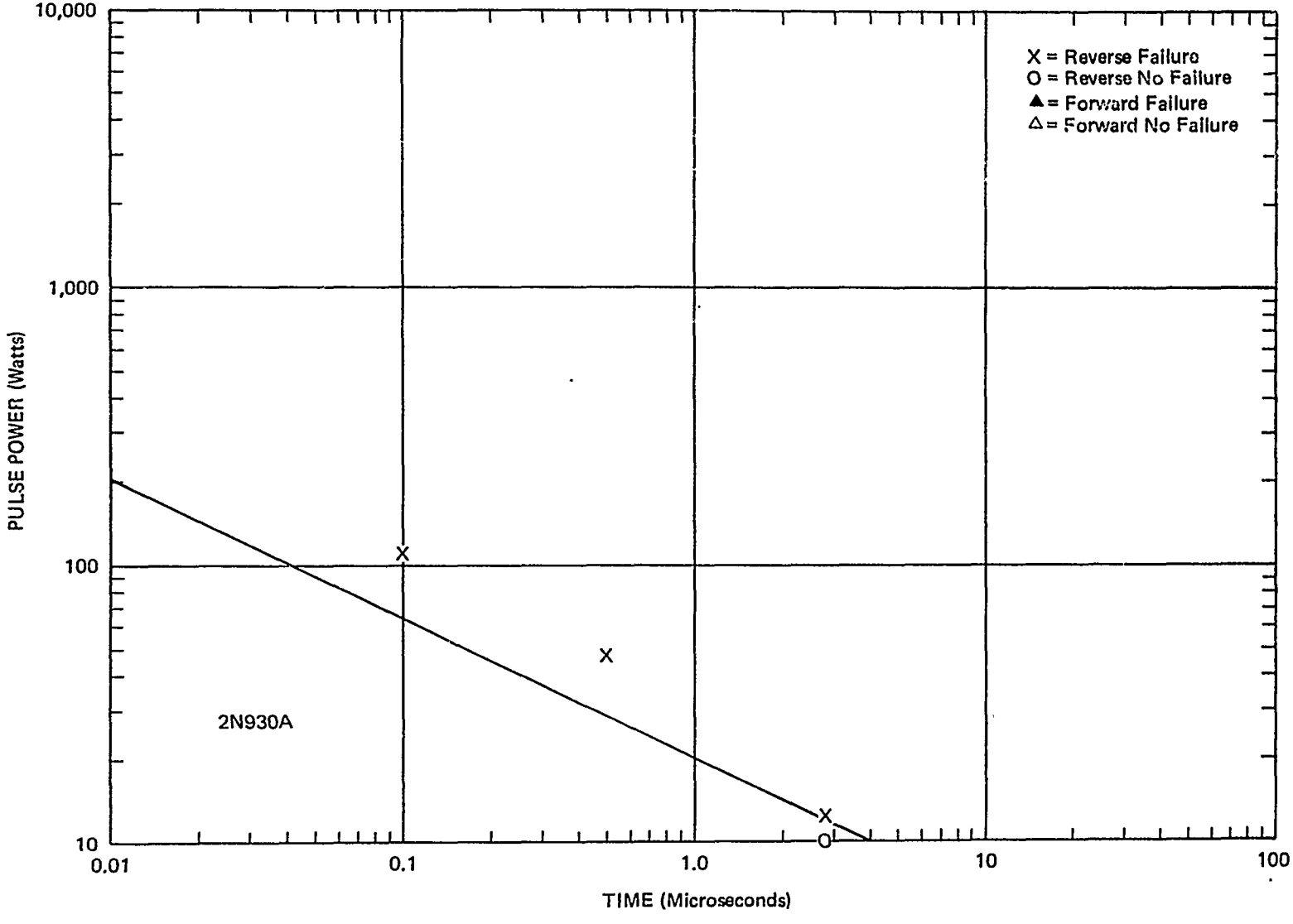

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N760A
(B–E)


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N927

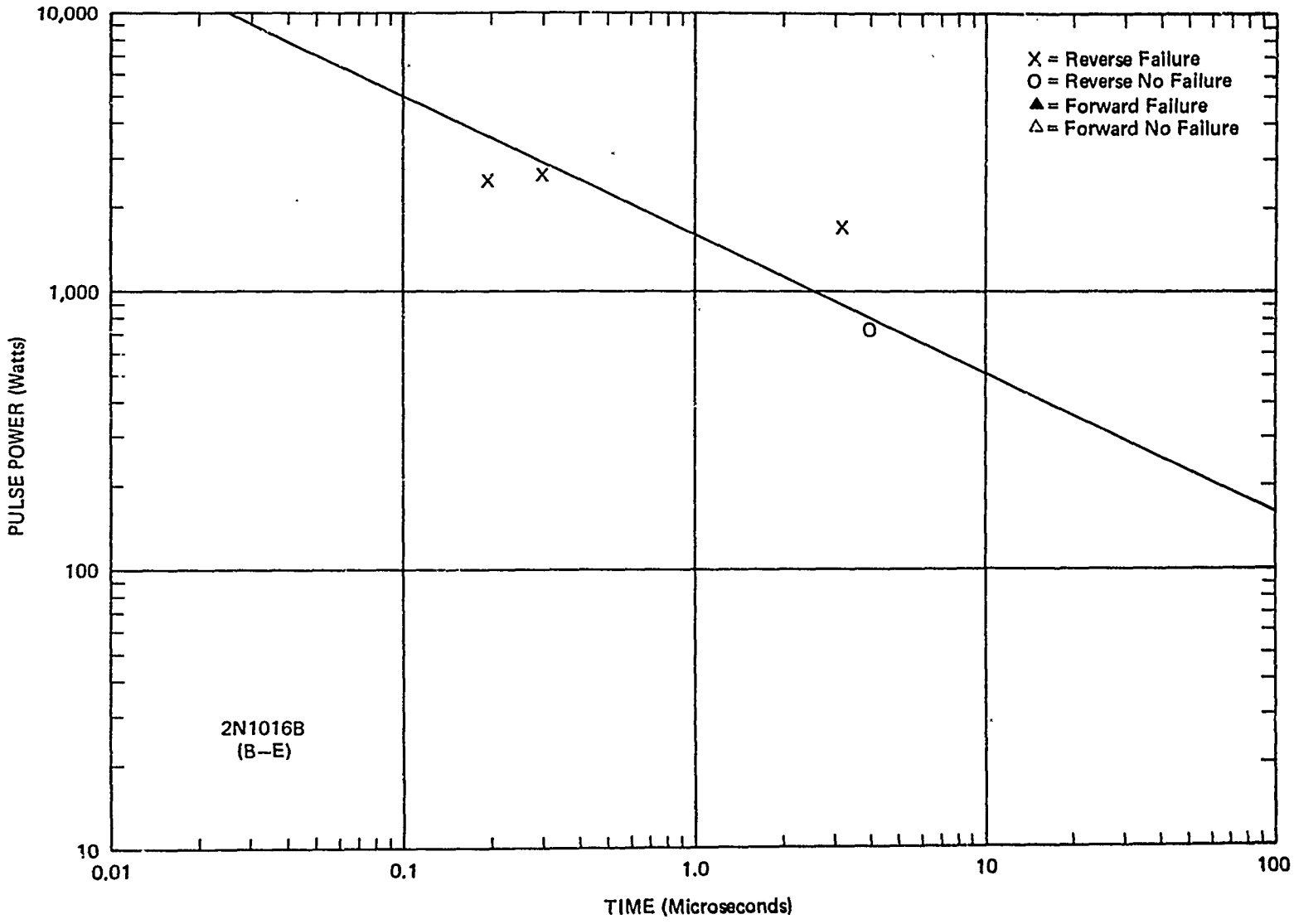
3.99


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N930
10588664–1
(B–E)

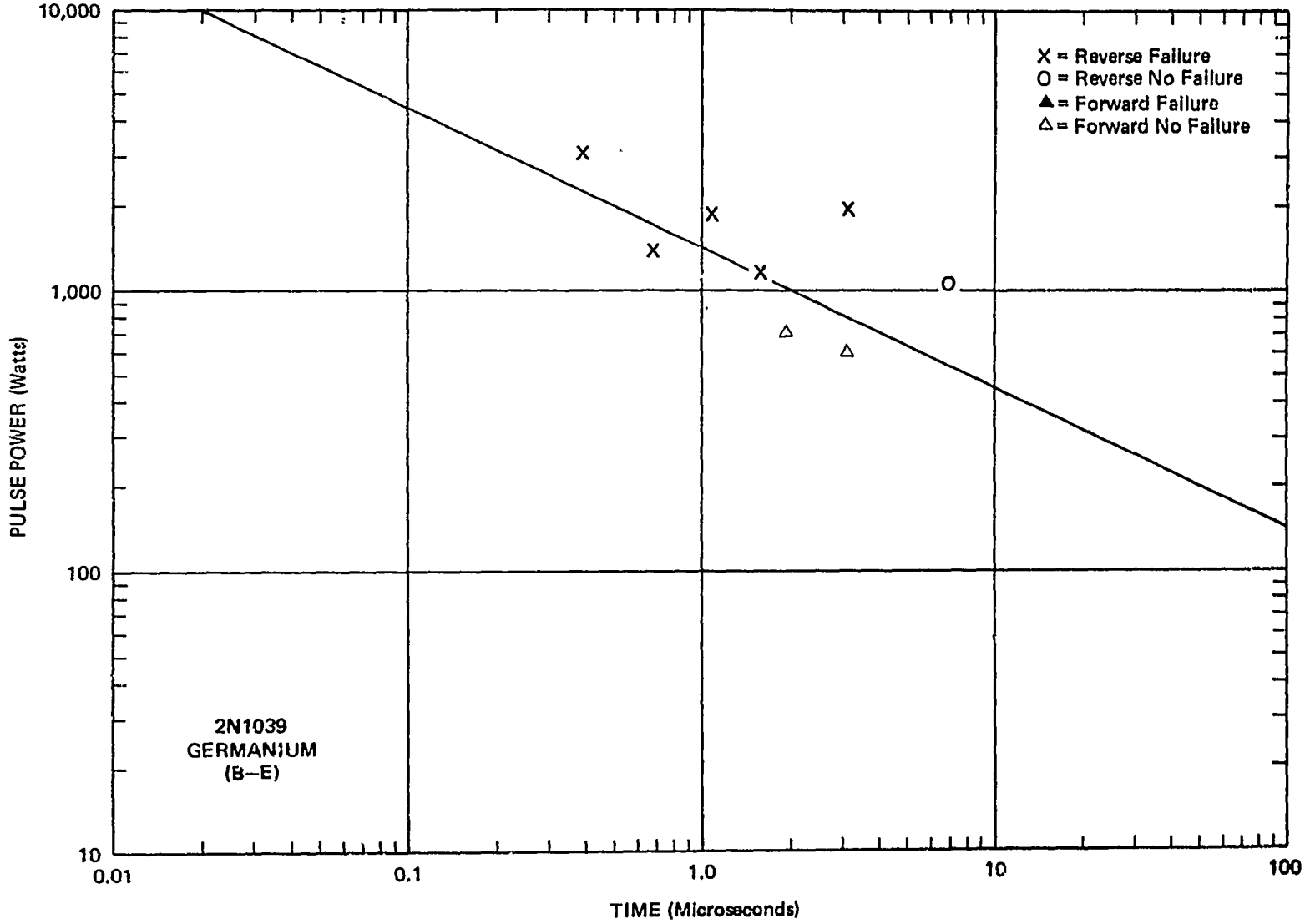
3.100

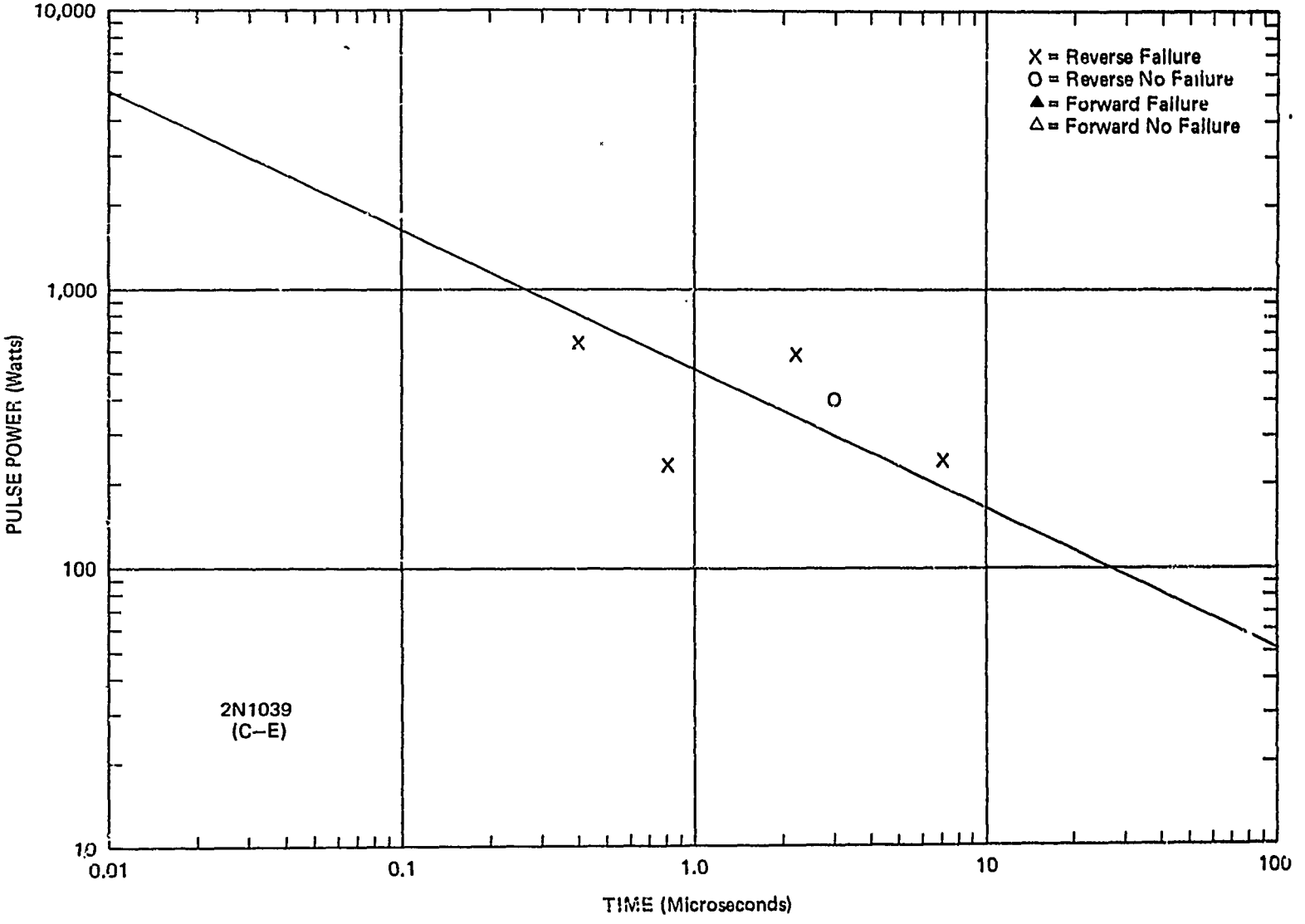

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N930A

3.101


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1016B
(B–E)

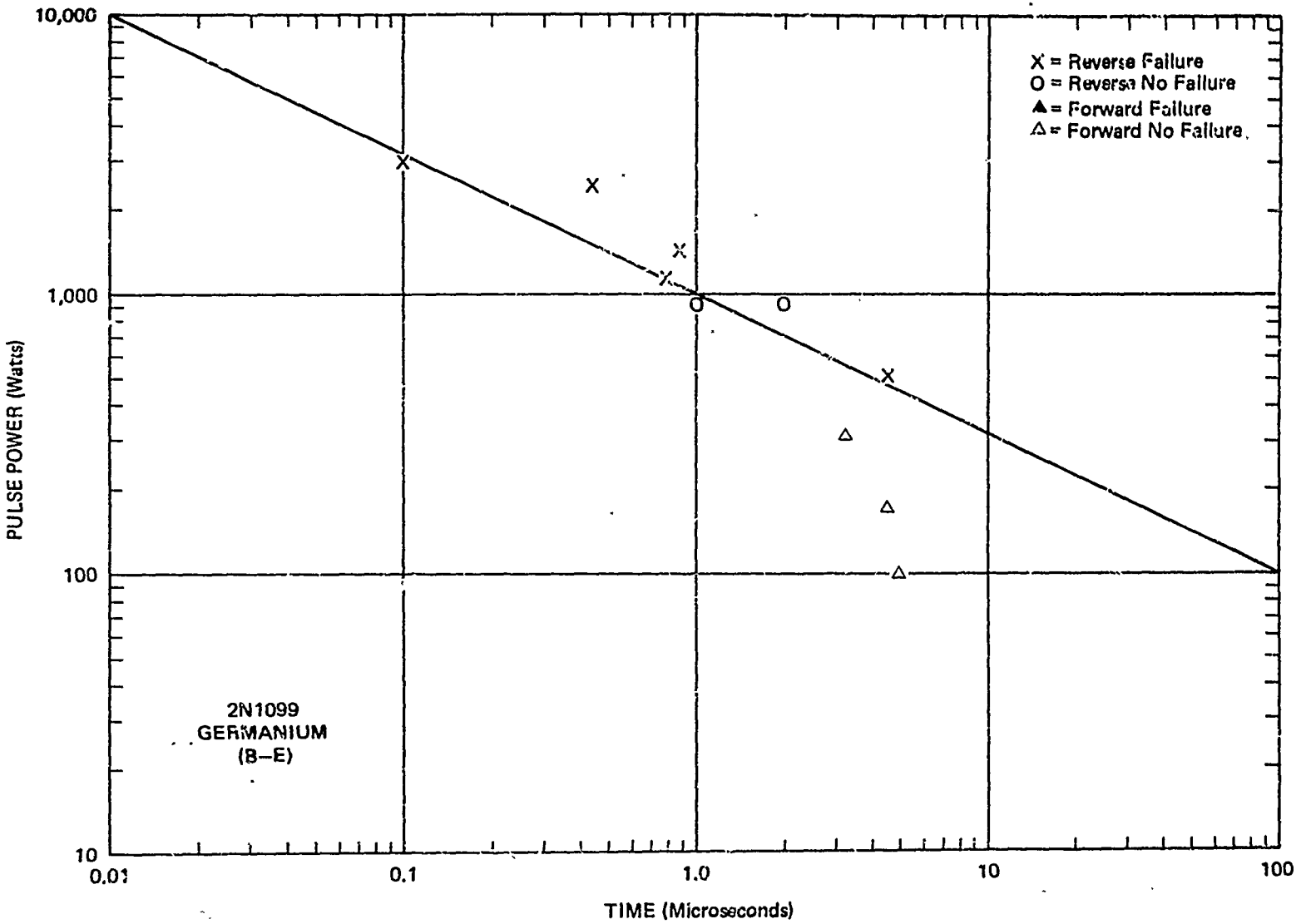
3.102


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1039
GERMANIUM
(B–E)

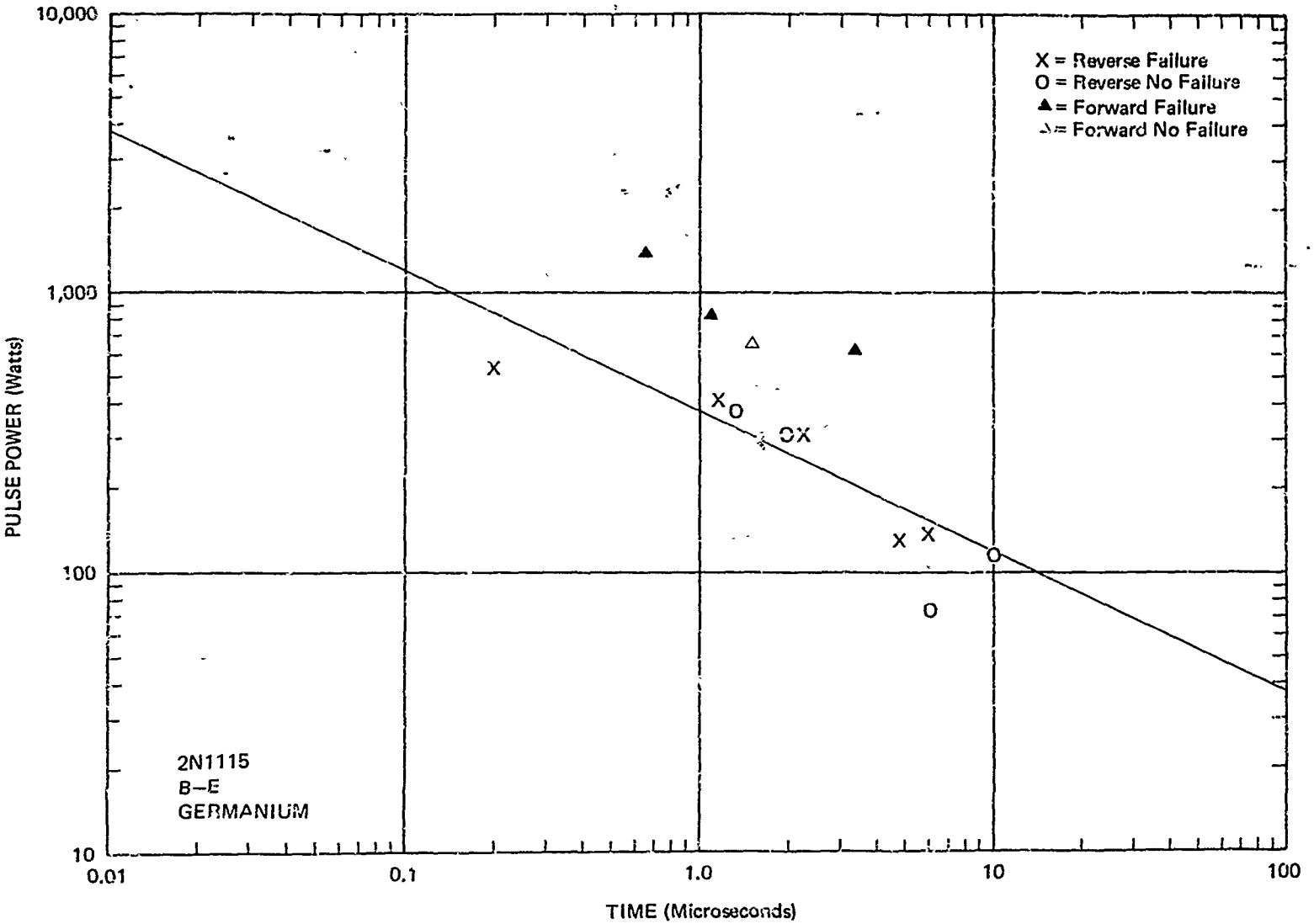

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1039
(C–E)

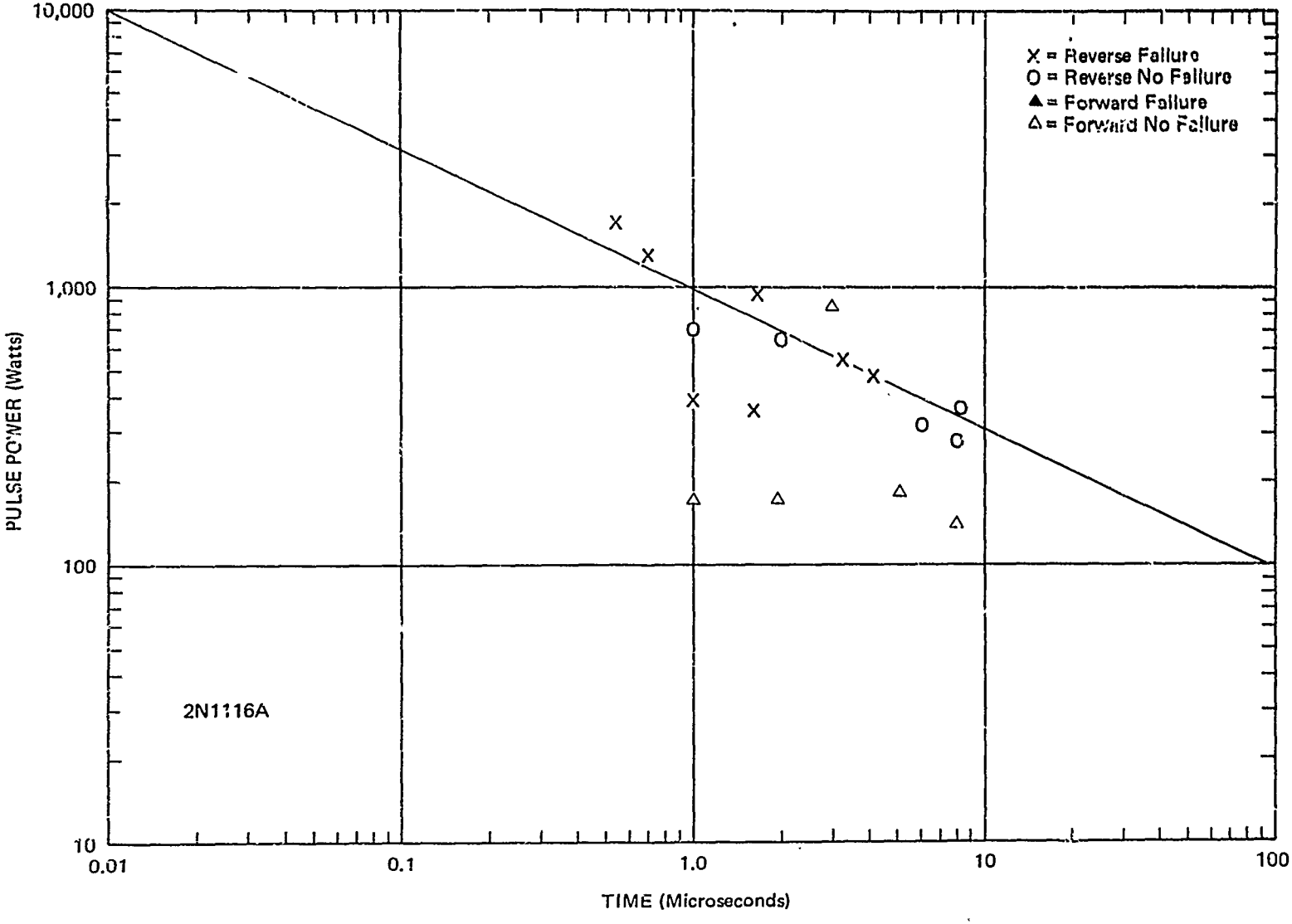
3.104

851

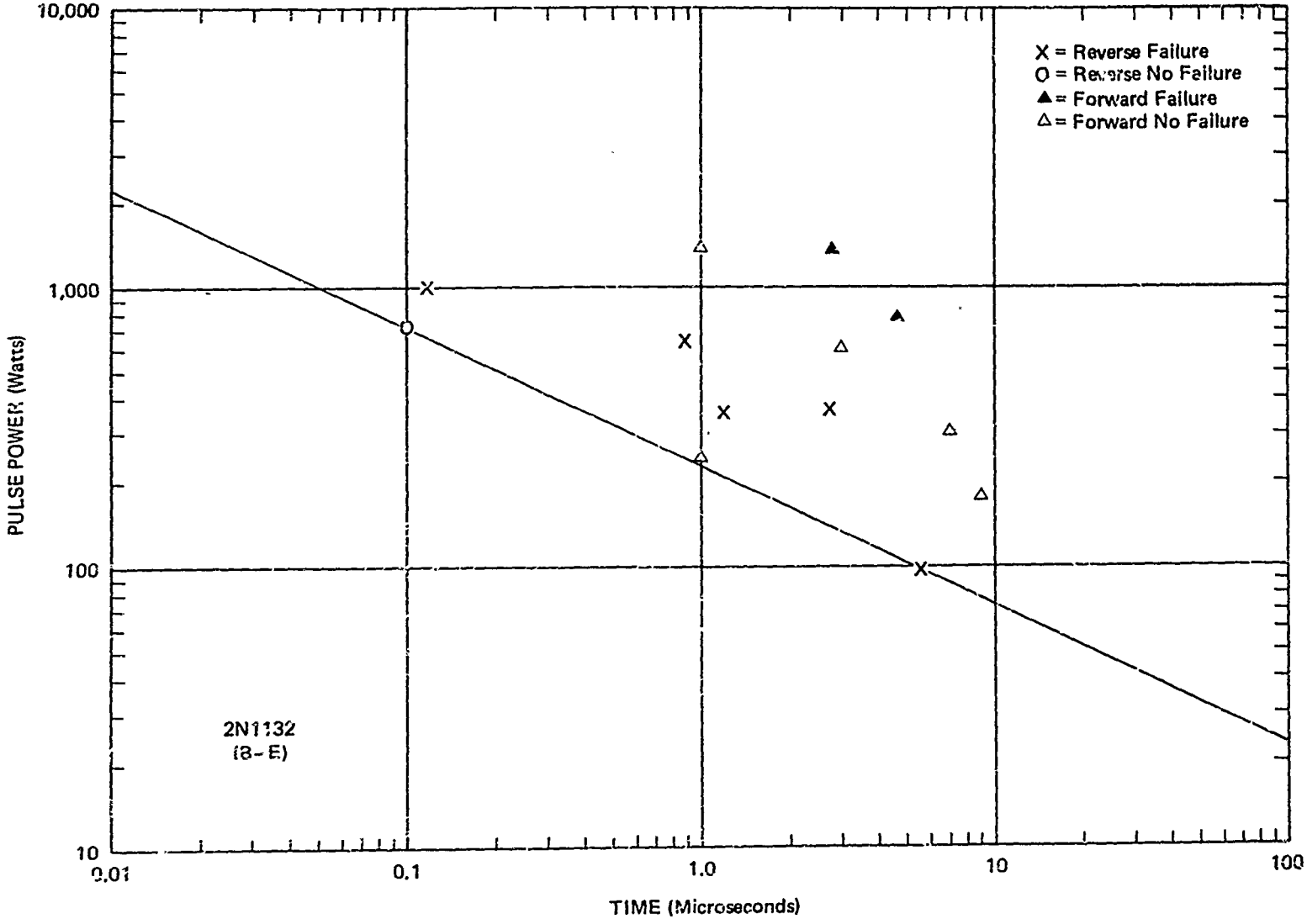

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1099
GERMANIUM
(B–E)

3.105


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1115
B–E
GERMANIUM

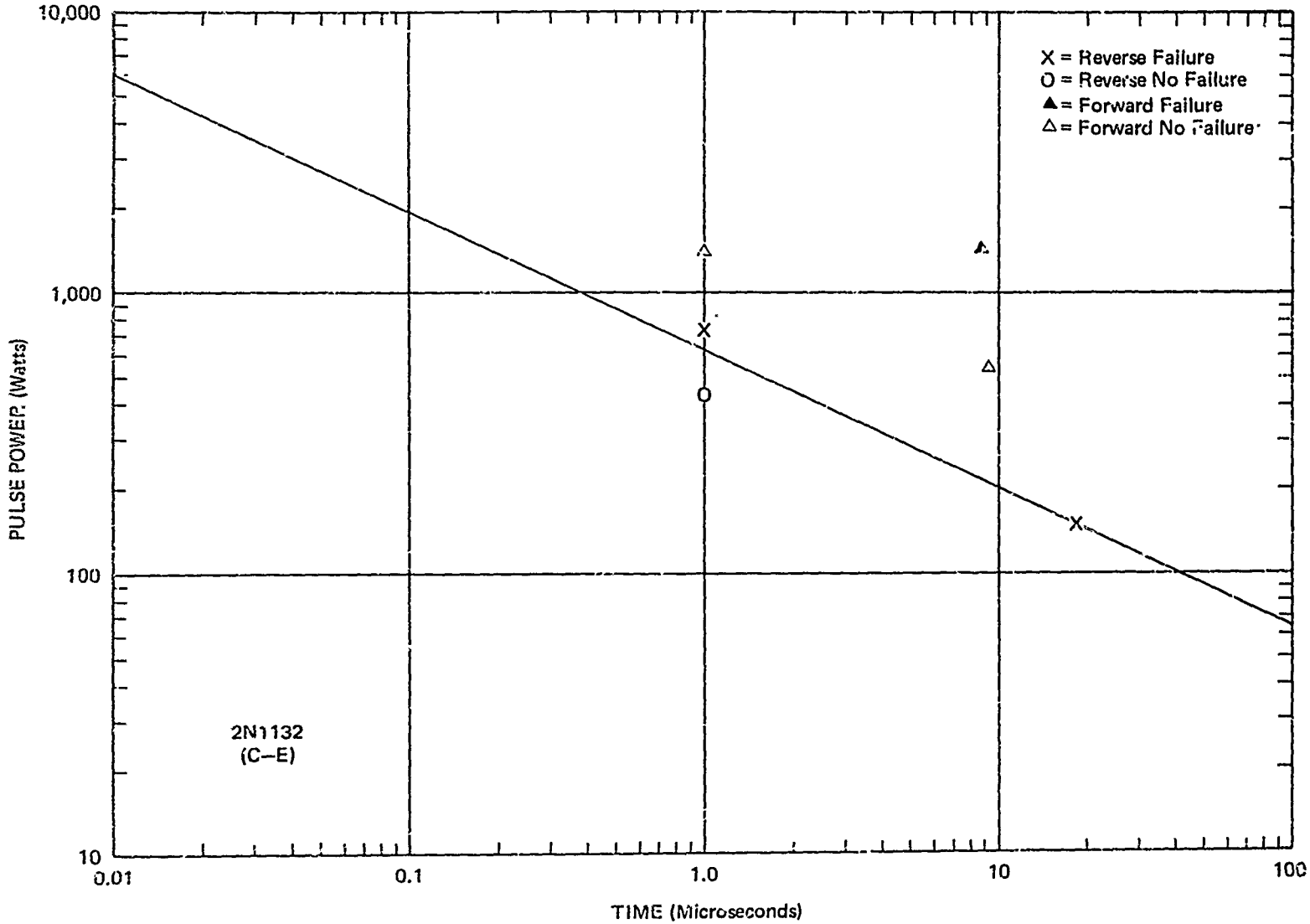

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1116A

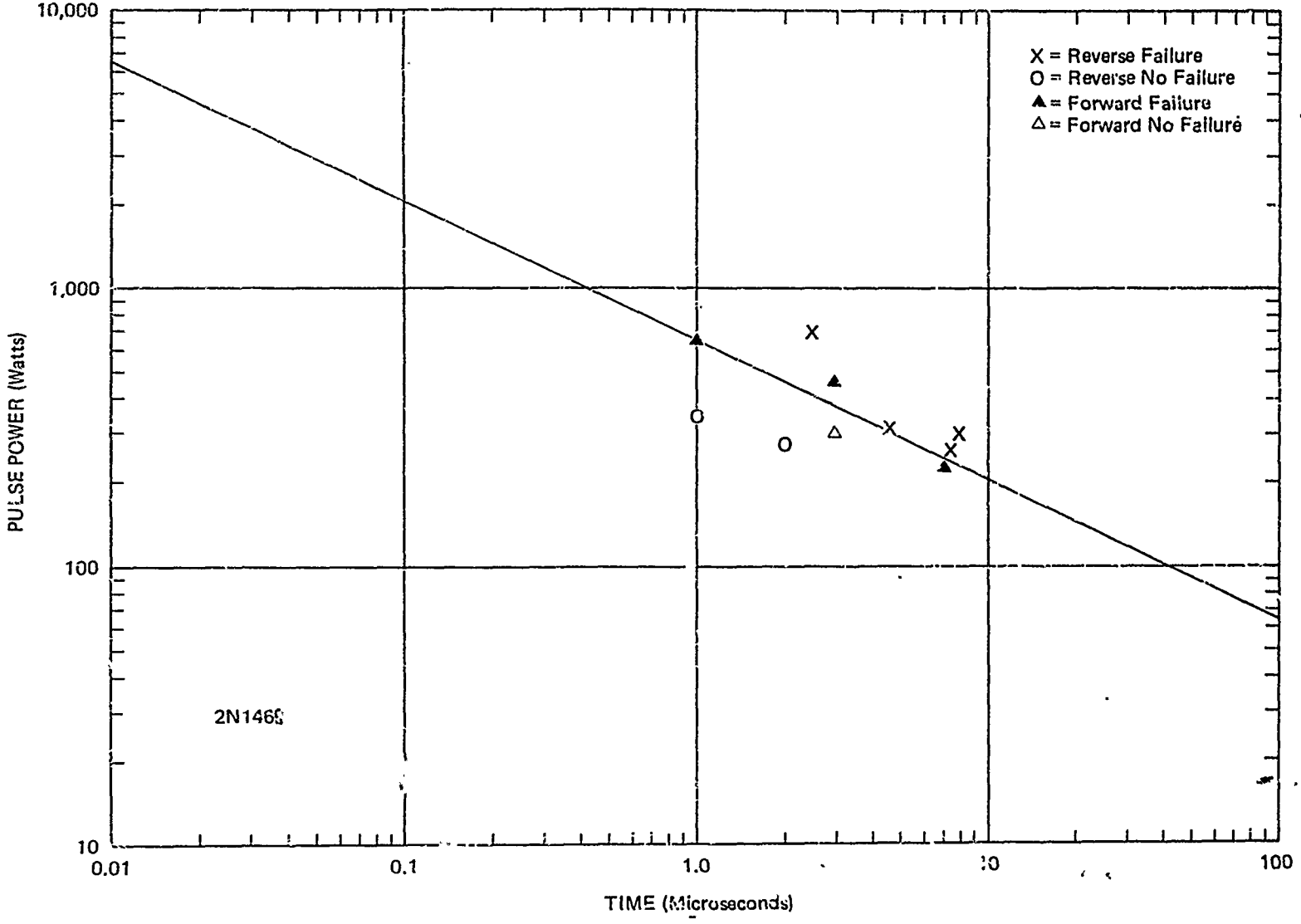
3.107

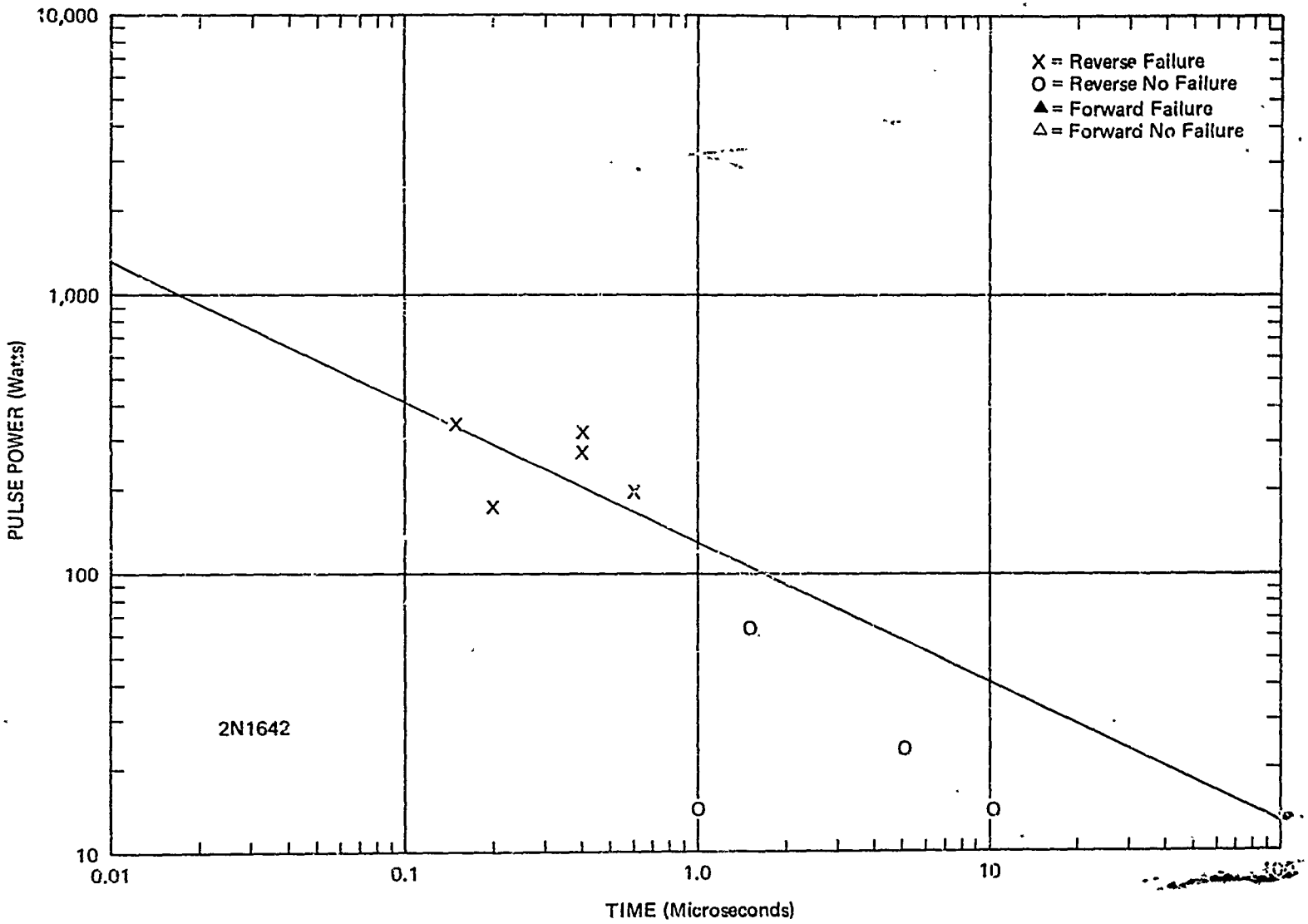

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1132
(8-E)

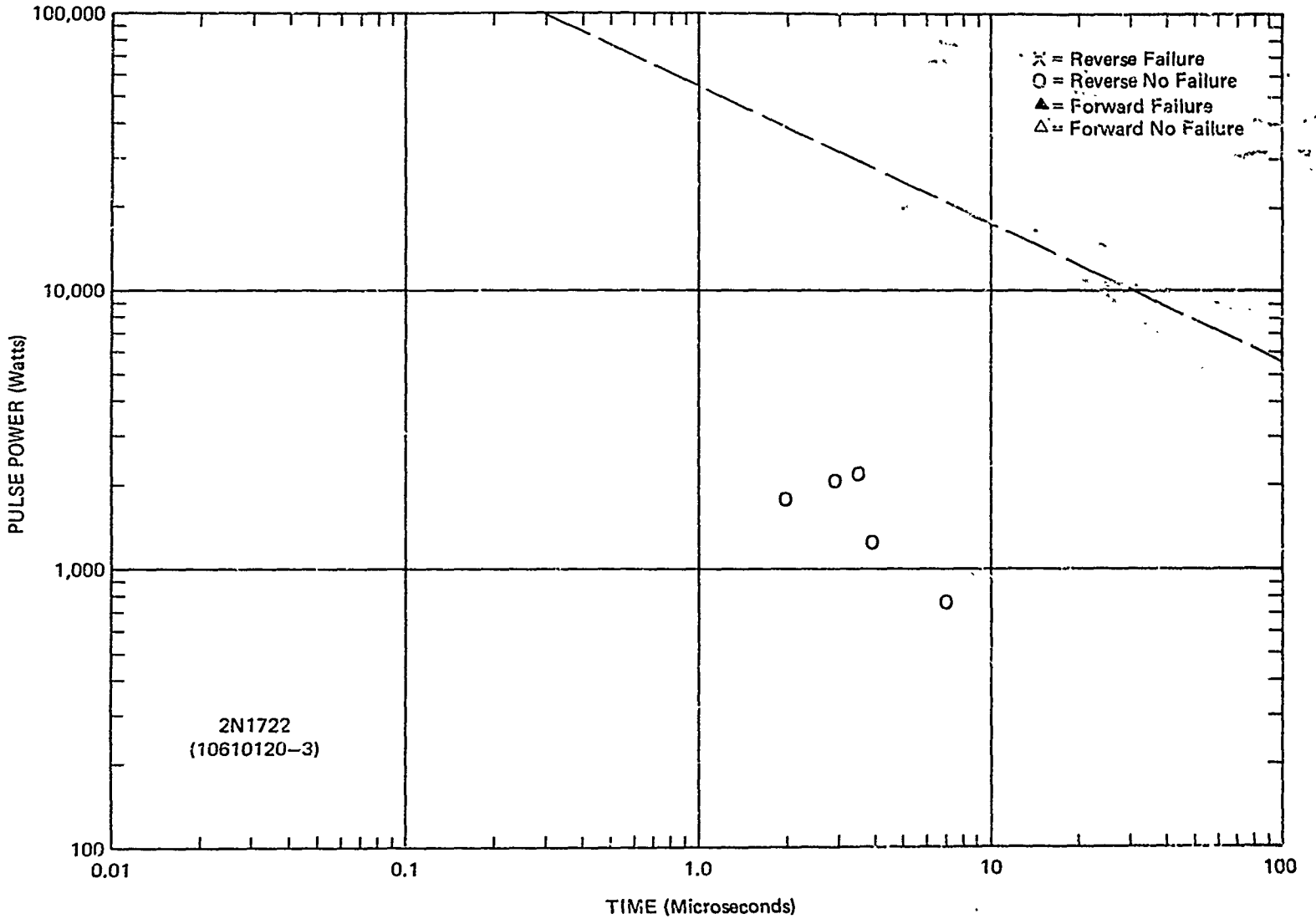
3.108

291

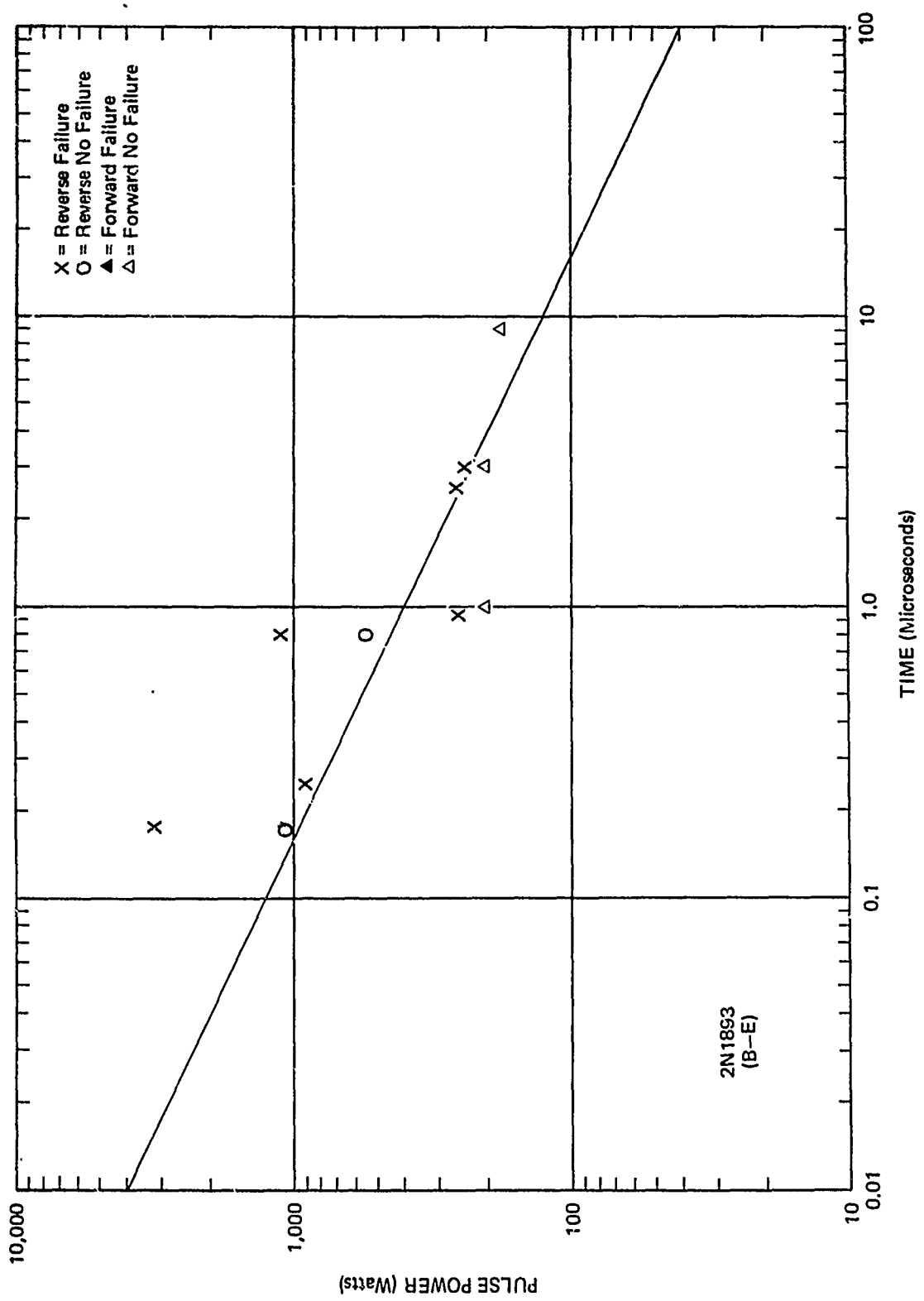

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1132
(C–E)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1469

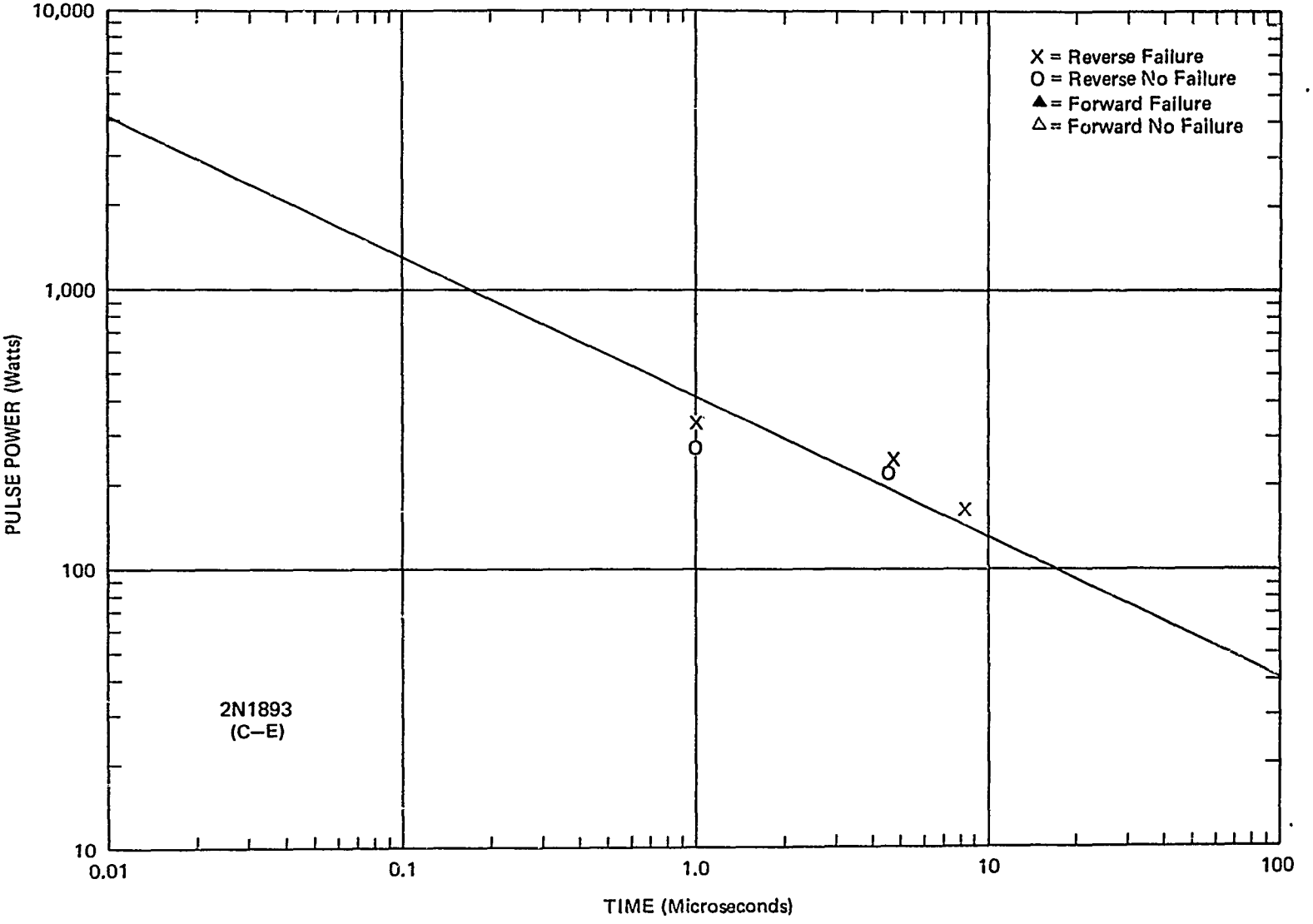

10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1642


100,000
10,000
1,000
100
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
= Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1722
(10610120–3)

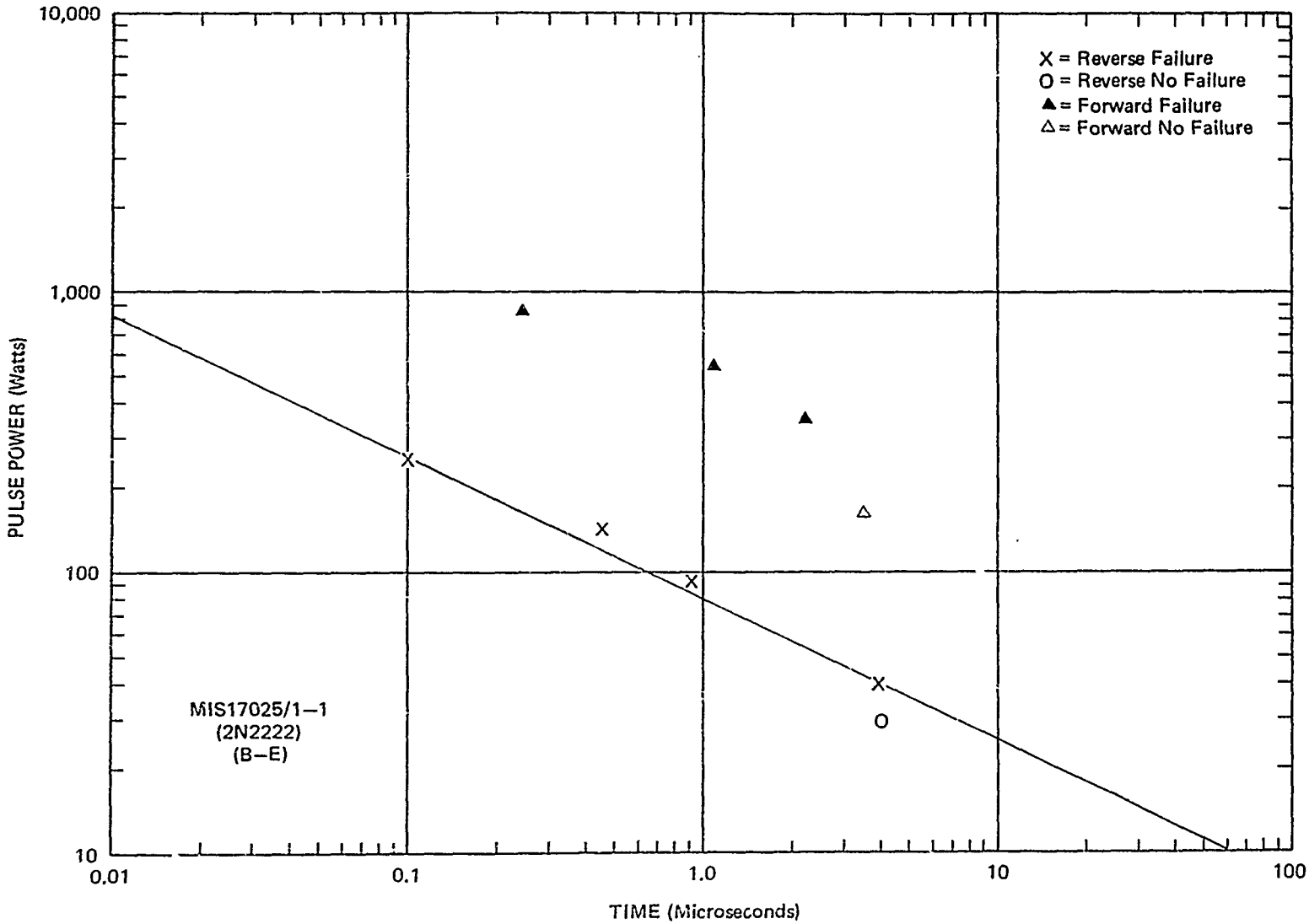
3.112

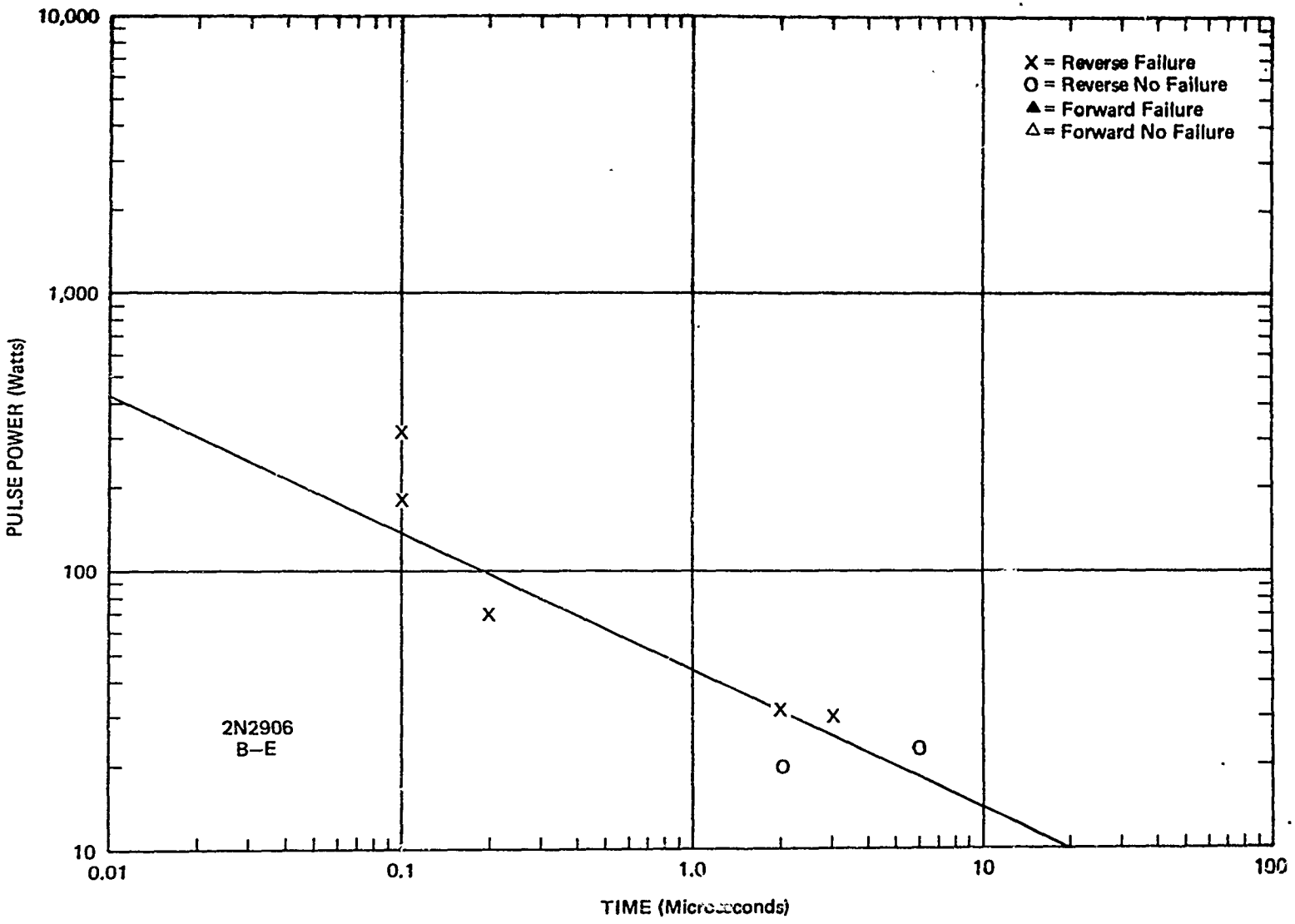

X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1893
(B–E)
PULSE POWER (Watts)
10,000
1,000
100
10
0.01
0.1
1.0
10
100
TIME (Microseconds)

3.113

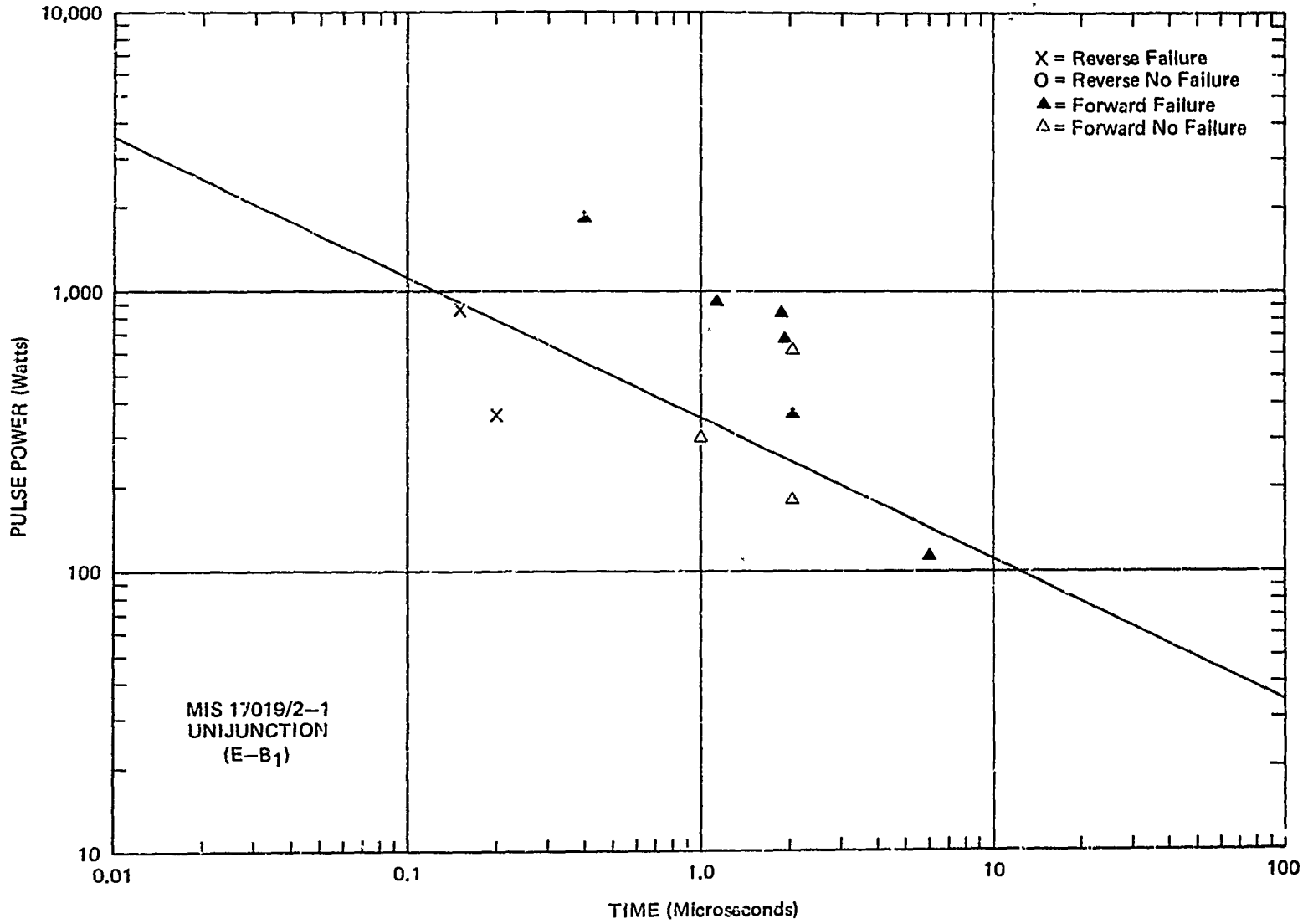

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N1893
(C–E)

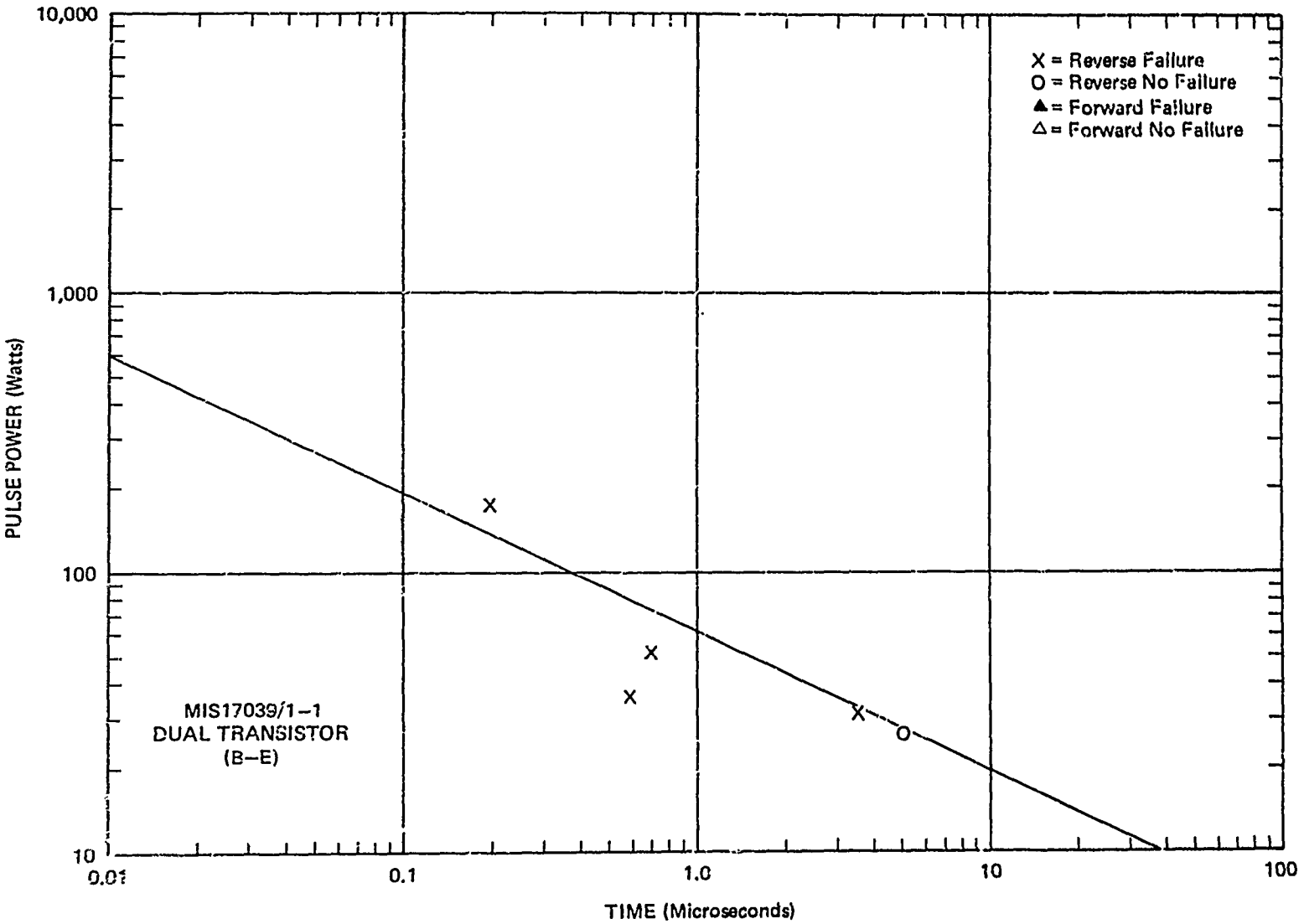
3.114


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17025/1–1
(2N2222)
(B–E)

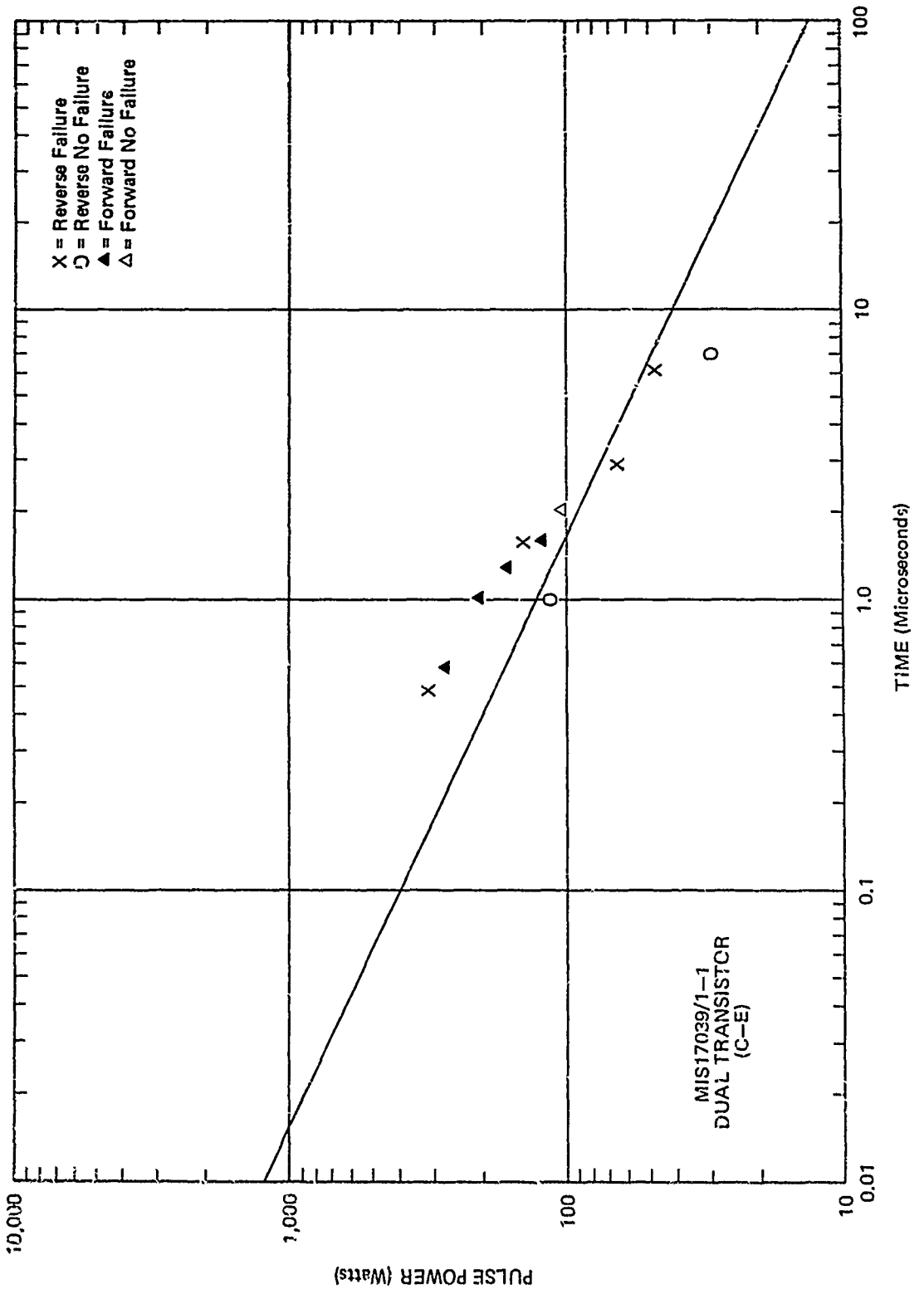

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2906
B–E

K′ = 0.044

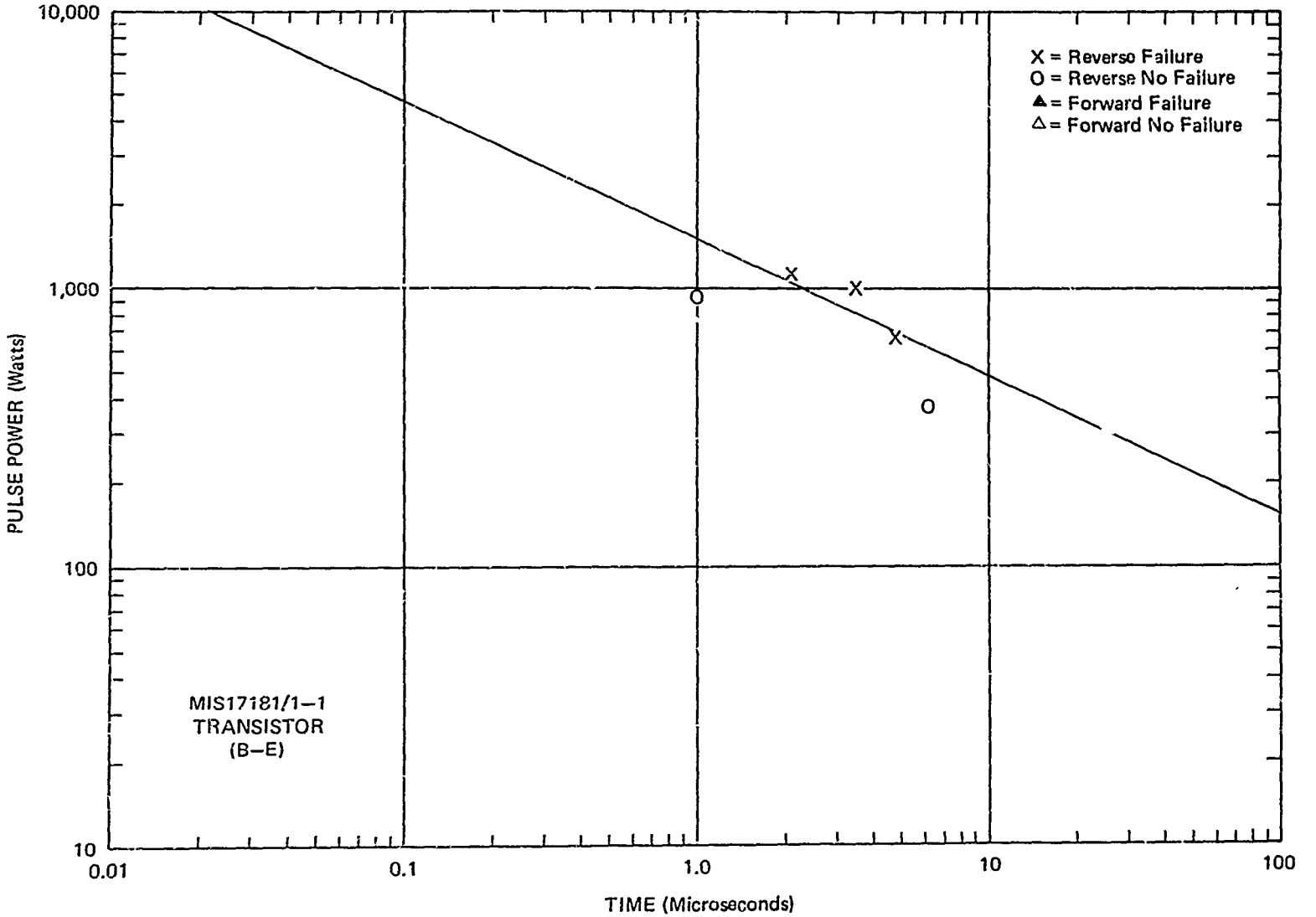

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17019/2–1
UNIJUNCTION
(E–B1)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17039/1-1
DUAL TRANSISTOR
(B-E)

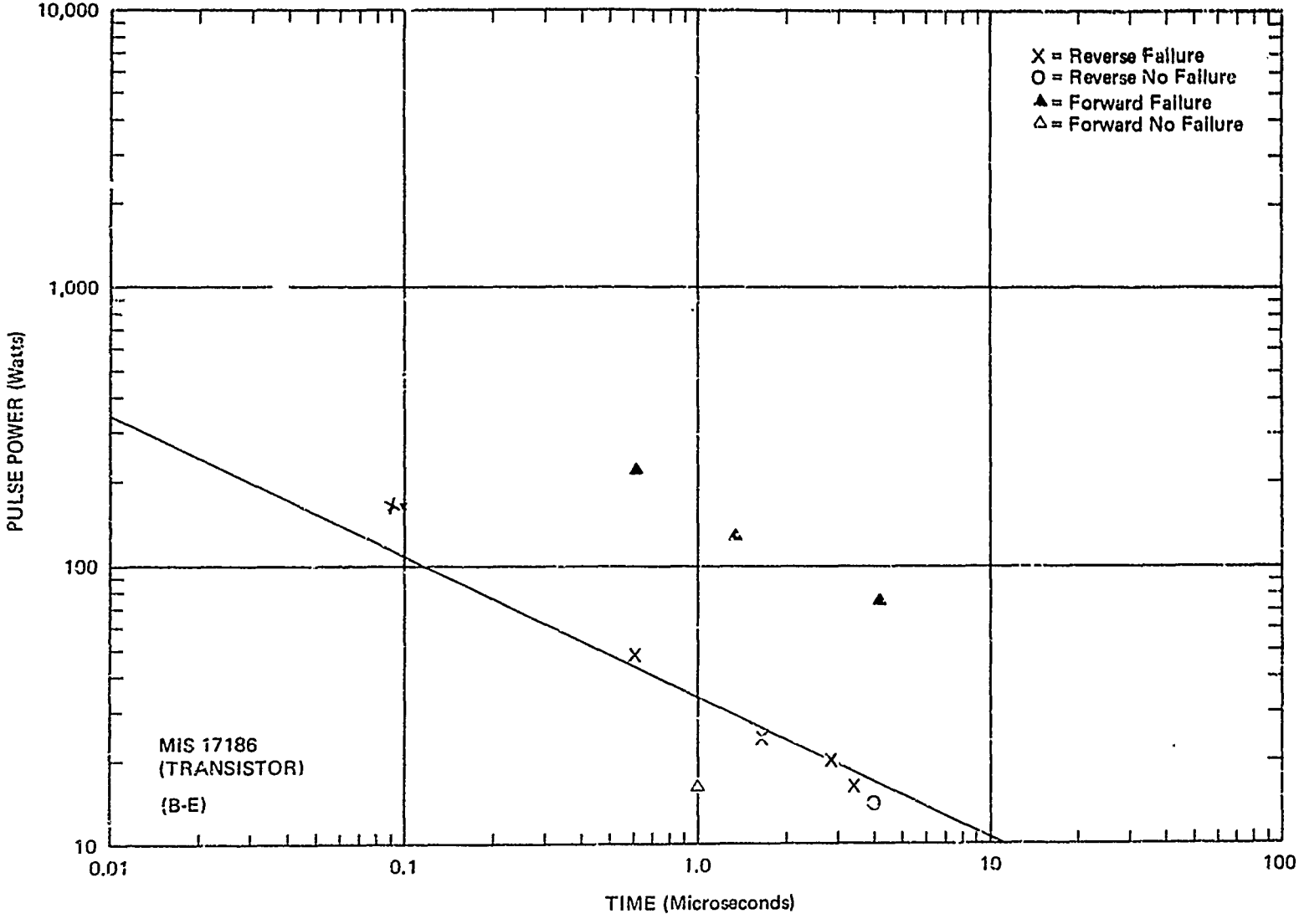
3.118


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17039/1-1
DUAL TRANSISTOR
(C-E)
PULSE POWER (Watts)
10,000
1,000
100
10
TIME (Microseconds)
0.01
0.1
1.0
10
100

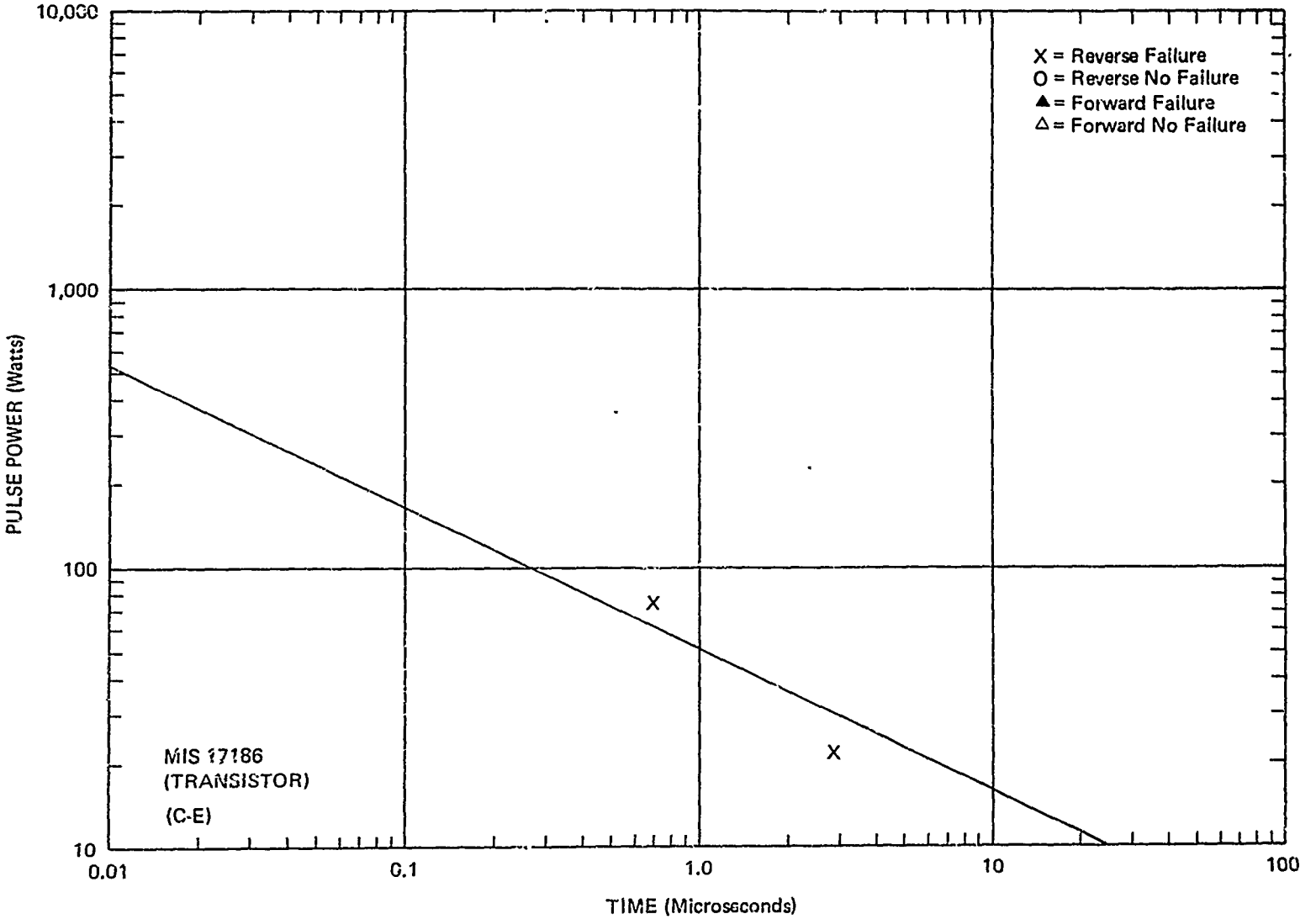
3.119

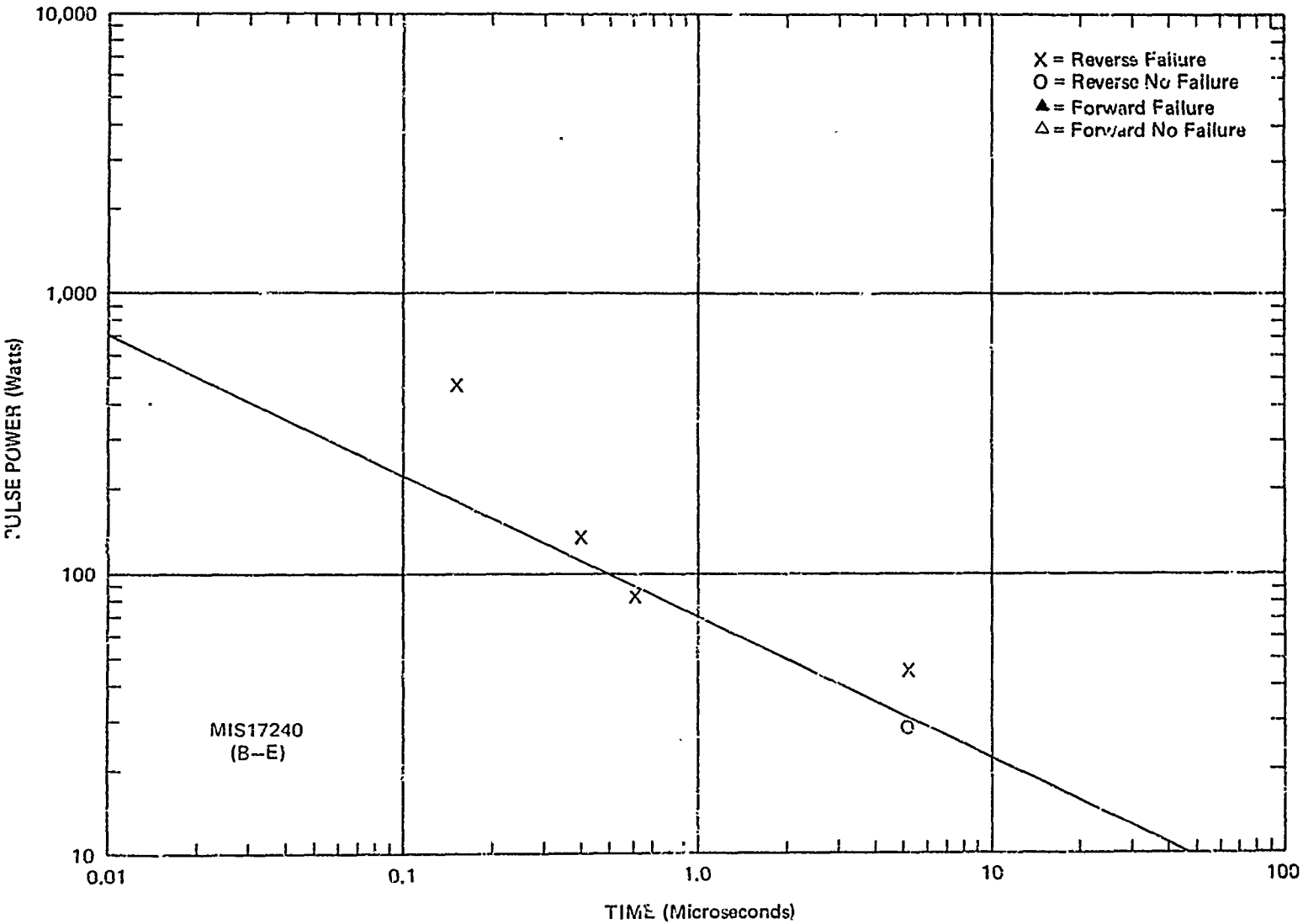

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17181/1–1
TRANSISTOR
(B–E)

3.120

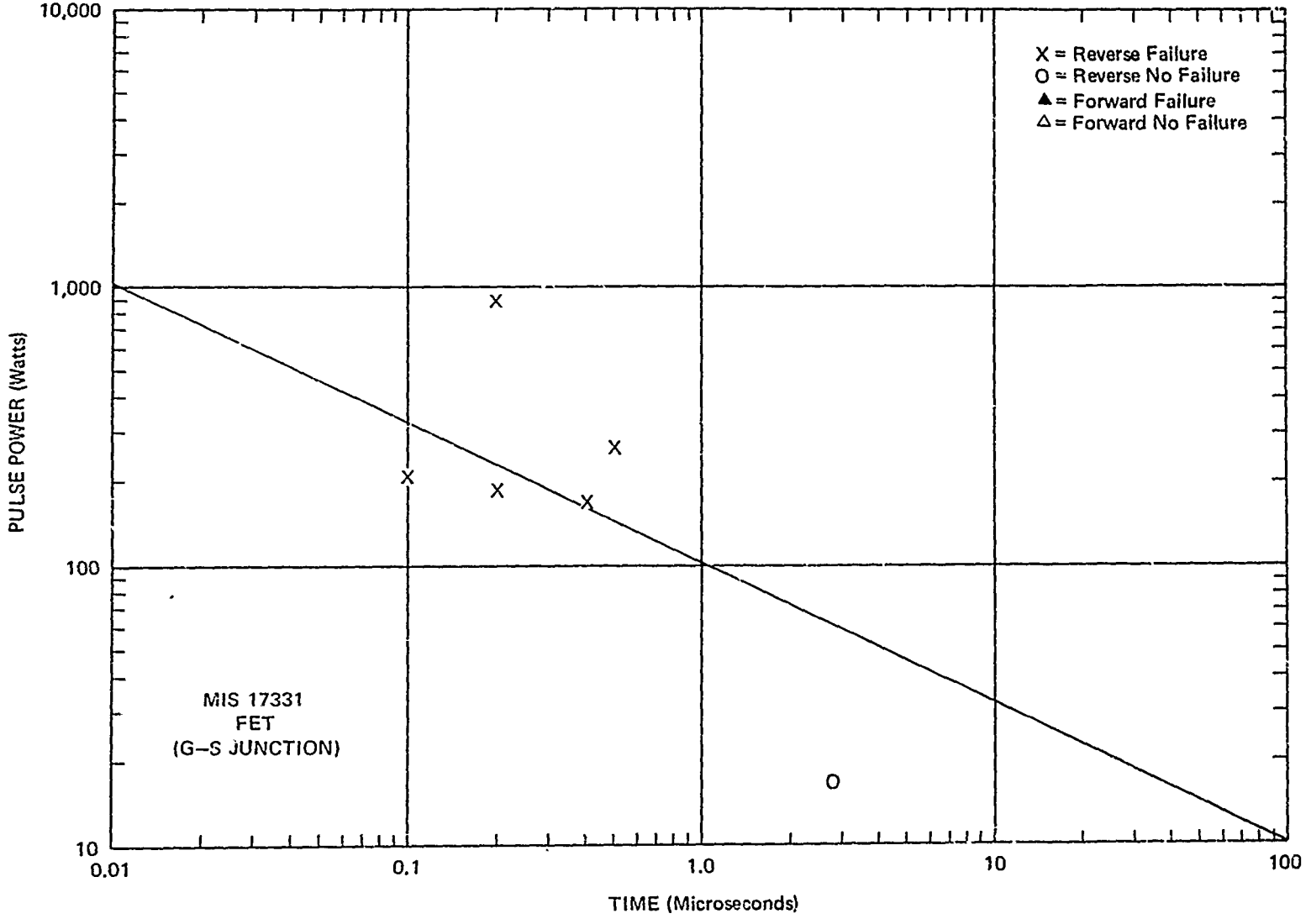

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17186
(TRANSISTOR)
(B-E)

3.121


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
X
X
MIS 17186
(TRANSISTOR)
(C-E)

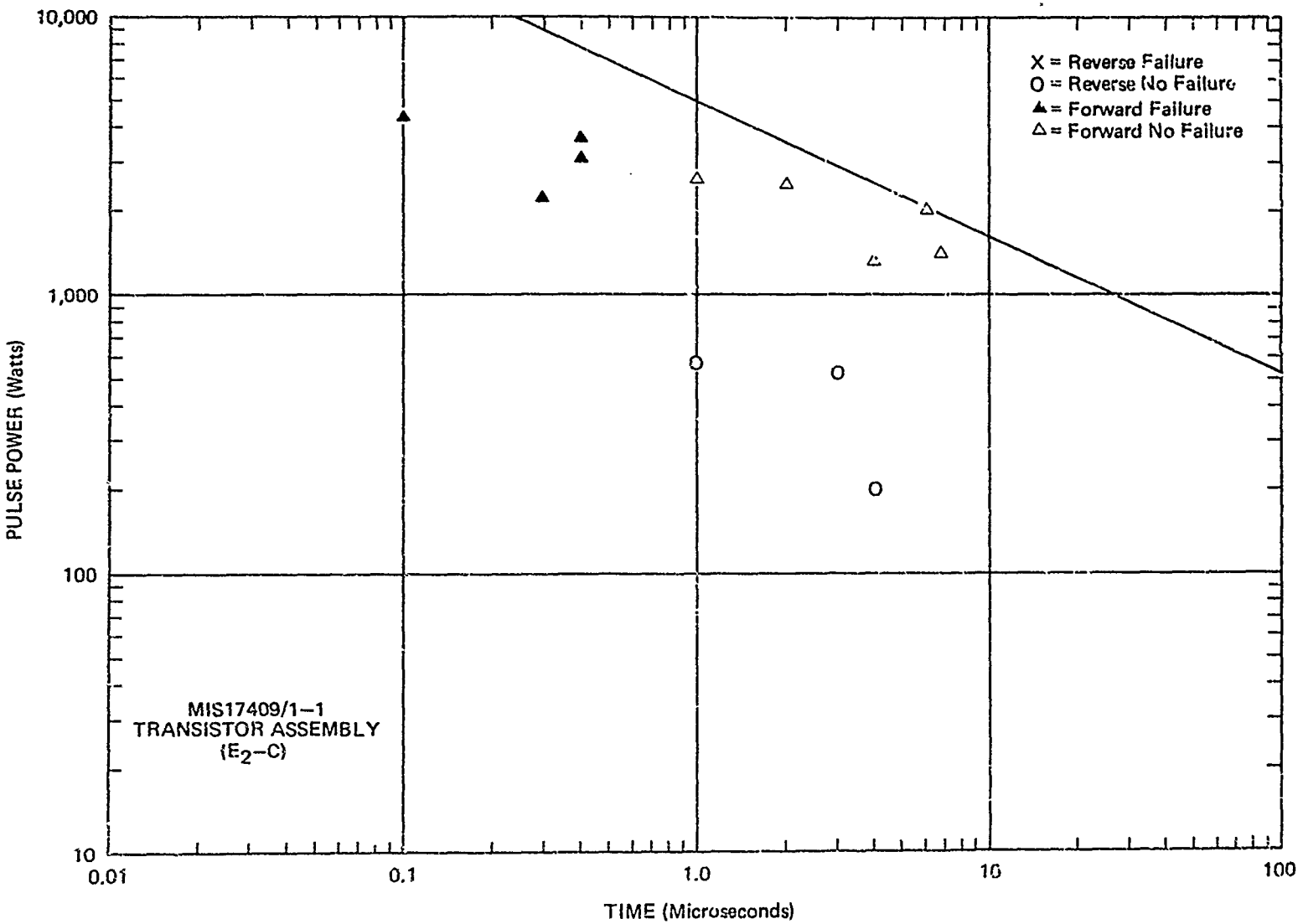

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17240
(B--E)

3.123

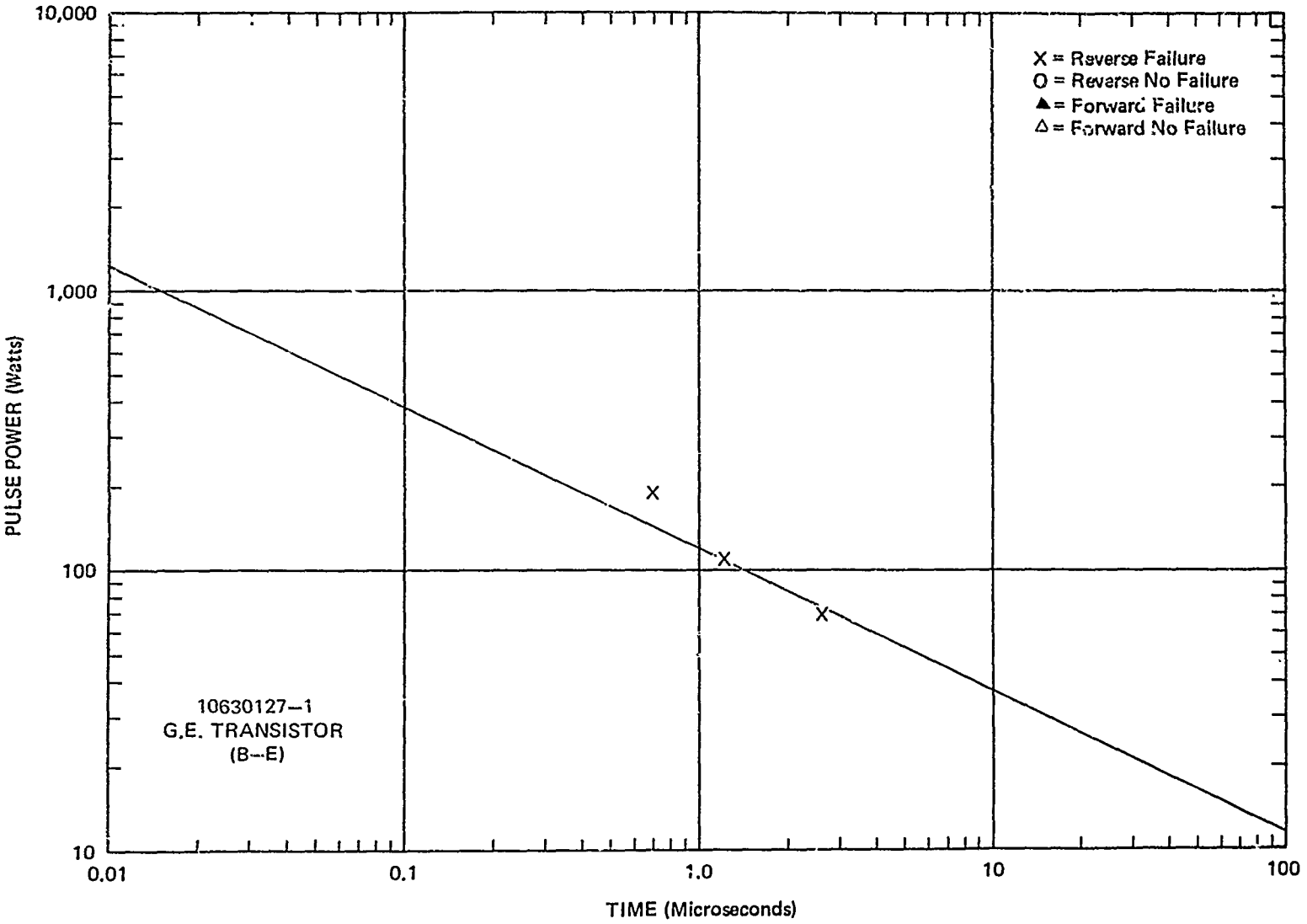

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS 17331
FET
(G–S JUNCTION)

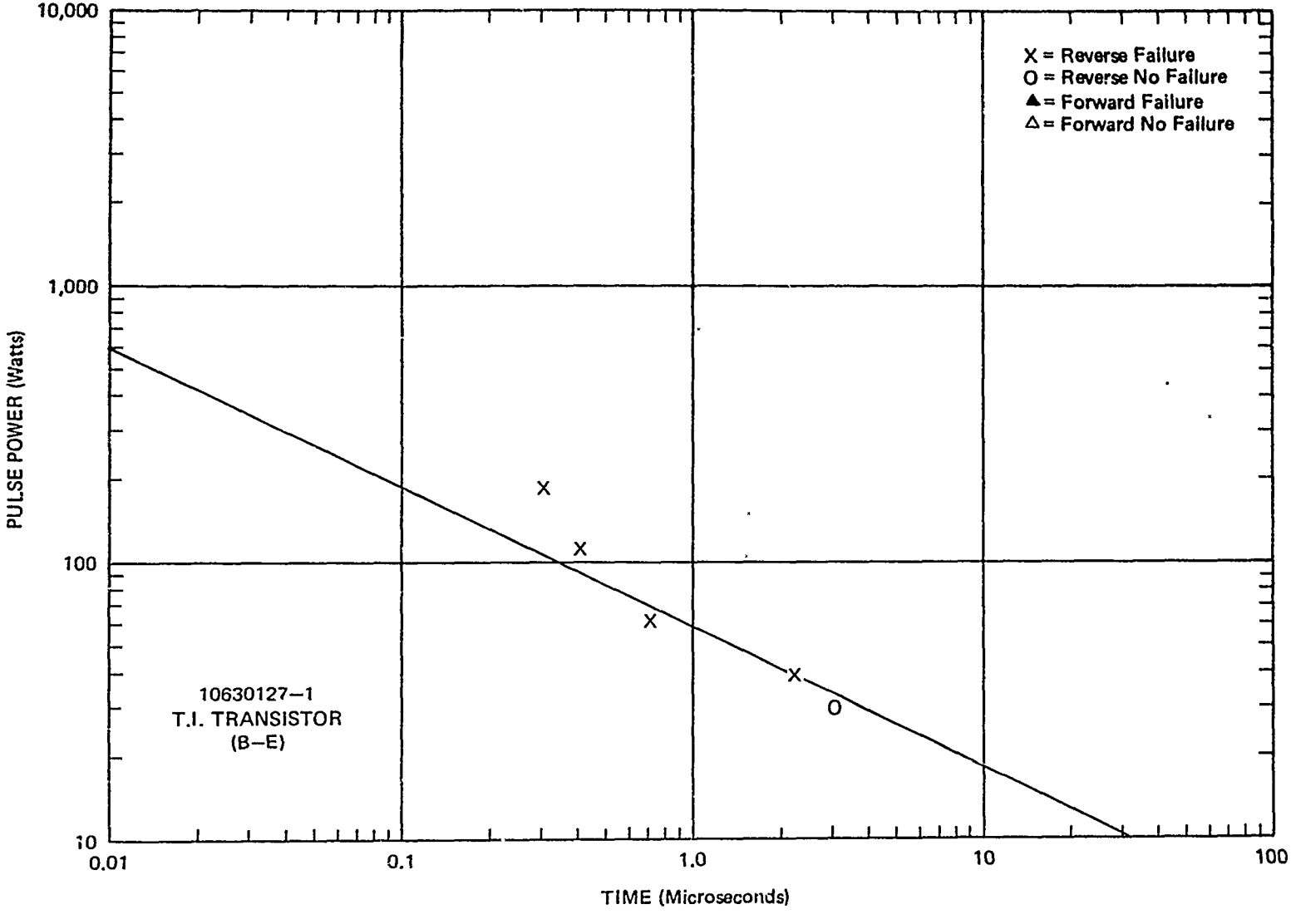
3.124

178

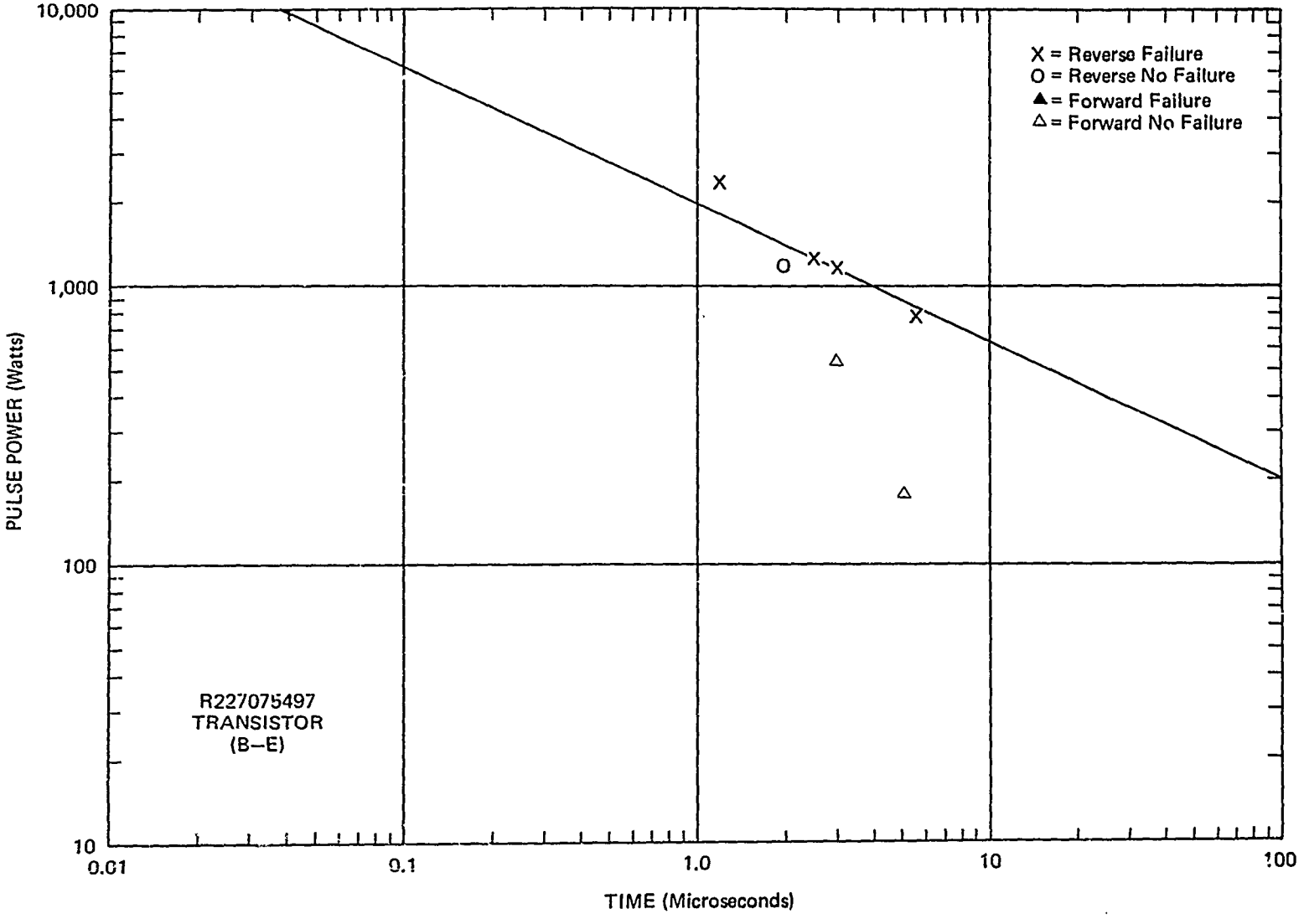

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MIS17409/1–1
TRANSISTOR ASSEMBLY
(E_2–C)

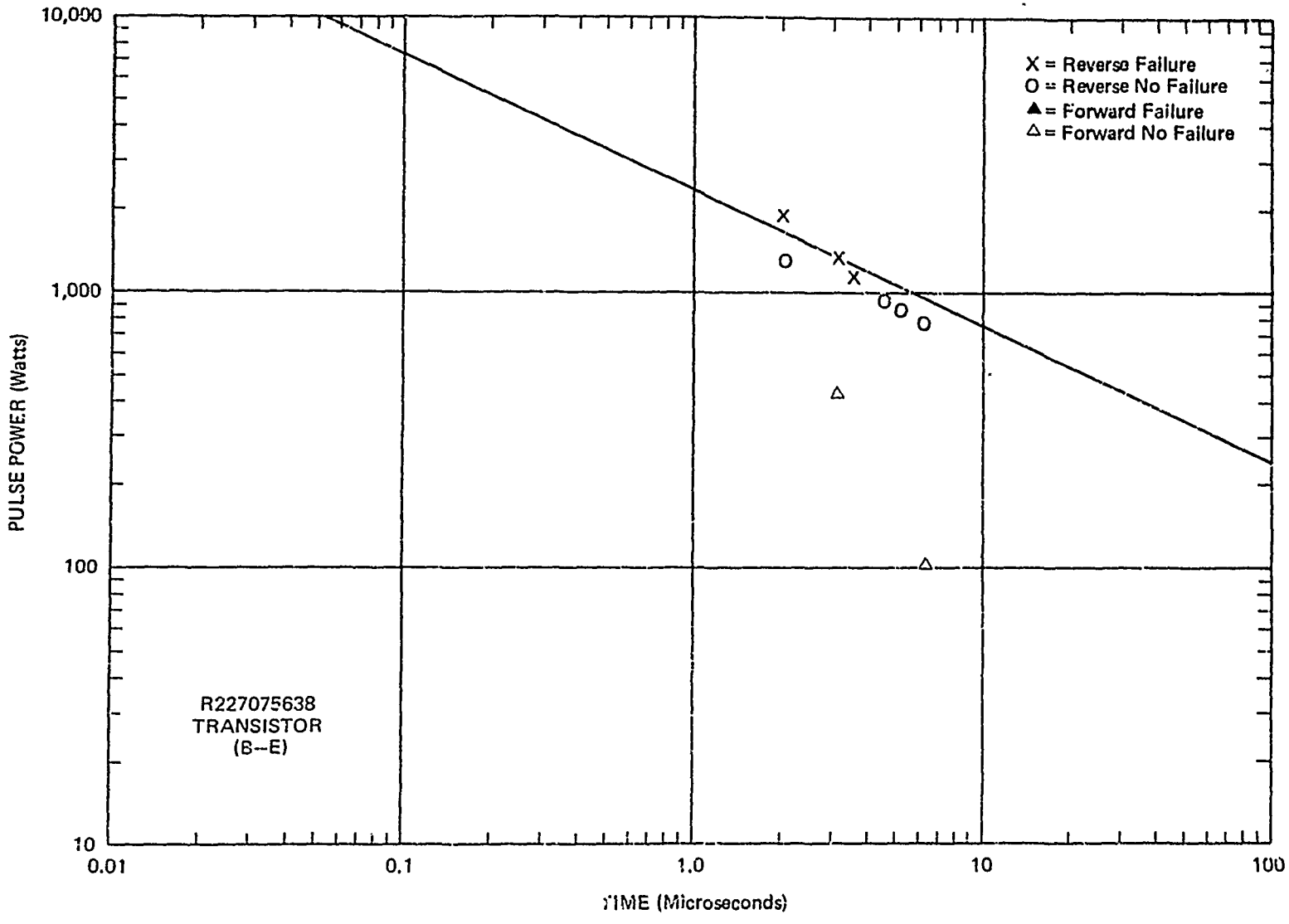
3.125


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
10630127–1
G.E. TRANSISTOR
(B–E)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
10630127–1
T.I. TRANSISTOR
(B–E)

3.127


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
R227075497
TRANSISTOR
(B–E)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
R227075638
TRANSISTOR
(B--E)

3.129

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K^1 (WATT-SEC$^{1/2}$)	JUNCTION AREA (CM^2)X10^{-3}	K^1/A $\left(\frac{\text{WATT-SEC}^{1/2}}{CM^2}\right)X10^3$
PT. CONTACT	1N82A	Sylvania		C-A	Yes	3	Yes	4	0.0007		
RECTIFIER	1N250B	G. E.	10630152-1	C-A	No	1	No	1	164.0*	293°	
RECTIFIER	1N253	G. E.		C-A	No	1	Yes	3	0.86	2.69°	0.32
RECTIFIER	1N338	Transitron	10629635	C-A	No	2	No	3	18.3*	32.6	
TEMP COMP	1N429	Dickson		C-A	Yes	3	No	1	6.5		
TEMP COMP	1N429	Hoffman		C-A	Yes	2	Yes	3	0.6		
TEMP COMP	1N429	I.R.C.		C-A	No	1	No	1	6.05*	10.9	
LOW LEVEL RECTIFIER	1N459	Transitron		C-A	No	1	Yes	5	0.59	2.83	0.208
LOW LEVEL RECTIFIER	1N459A	C. R. L.		C-A	No	1	Yes	3	0.96	0.835	1.15
LOW LEVEL RECTIFIER	1N482A	Sylvania		C-A	No	1	Yes	5	0.96	1.37	0.701
RECTIFIER	1N536	G. E.		C-A	No	1	No	1	1.51*	2.69°	
RECTIFIER	1N537	G. E.		C-A	No	1	Yes	5	0.51	2.69°	0.189
RECTIFIER	1N540	G. E.		C-A	No	1	Yes	4	0.93	2.69°	0.346
RECTIFIER	1N645	G. I.		C-A	No	1	No	4	2.82*	5.12	
RECTIFIER	1N647	G. I.		C-A	No	2	No	3	2.82*	5.12	
RECTIFIER	1N649			C-A	No	2	No	2	2.86*	5.12	
ZENER	1N702A	Transitron	10630231	C-A	No	1	Yes	3	1.0	1.62°	0.618
ZENER	1N705A	Transitron		C-A	No	1	No	1	0.908*	1.62°	
ZENER	1N711A	C. R. L.	10630161-7	C-A	No	1	Yes	3	2.1	1.6	1.312

* ESTIMATED

° MANUFACTURER'S QUOTE

TABLE I

SEMICONDUCTOR DAMAGE RESULTS FOR DIODES & SCR'S (PERSHING).

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K' (WATT-SEC$^{1/2}$)	JUNCTION AREA (CM^2)X10^{-3}	$K'/A\left(\frac{\text{WATT-SEC}^{1/2}}{\text{CM}^2}\right)\times 10^3$
ZENER	1N751A	T. I.		C-A	No	1	No	2	1.13*	2.03°	
ZENER	1N752A	T. I.		C-A	No	1	No	1	1.13*	2.03°	
ZENER	1N753A	T. I.		C-A	No	1	Yes	5	1.2	2.03°	0.592
ZENER	1N763-2	Transitron	10587417-3	C-A	No	1	No	1	1.77*	3.16	
STABISTOR	1N816	Transitron	10587418-1	C-A	No	1	Yes	4	1.5	1.62°	0.926
ZENER	1N823	Transitron		C-A	No	2	Yes	6	1.8	2.59°	0.695
SWITCHING	1N933J	Erie Tech.	10607918-1	C-A	No	0	Yes	4	0.1		
TEMP COMP	1N939A	Dickson		C-A	No	2	No	1	6.95*	12.4	
ZENER	1N967B	Continental		C-A	Yes	2	Yes	3	0.73	0.61	1.196
ZENER	1N981B	Dickson		C-A	No	1	Yes	6	1.4	2.29	0.612
RECTIFIER	1N1095	G.E.		C-A	No	1	Yes	6	0.88	2.69°	0.327
RECTIFIER	1N1342A	Westinghouse		C-A	No	1	No	1	44.3*	79.1°	
RECTIFIER	1N1585	Transitron		C-A	No	1	No	1	3.5*	6.25	
ZENER	1N1770A	C. R. L.	10627724-1	C-A	No	3	No	3	14.2*	25.4	
ZENER	1N1783	Hoffman	10627719-1	C-A	No	2	No	2	21.3*	38.0	
TUNNEL	1N2929A	Hoffman	11040282-1	C-A	Yes	3	Yes	5	0.073	0.34	0.214
ZENER	1N3016B	Dickson		C-A	No	1	No	1	19.5*	34.8	
RECTIFIER	1N4816	Westinghouse		C-A	No	1			9.8*	17.5°	
RECTIFIER	1N4817	Westinghouse		C-A	No	1	No	1	9.8*	17.5°	

TABLE I (Continued)

SEMICONDUCTOR DAMAGE RESULTS FOR DIODES & SCR's (PERSHING).

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K^1 (WATT-SEC$^{1/4}$)	JUNCTION AREA ($CM^2 X 10^{-3}$)	$K^1/A \left(\frac{\text{WATT-SEC}^{1/4}}{CM^2}\right) X 10^3$
ZENER	983B649P2	Transitron		C-A	No	1	Yes	5	3.9	3.08	1.21
RECTIFIER	998A562G12	G. E.		C-A	No	1	No	2	58*	104	
DIODE BRIDGE	983B615-2	G. E.		C-A	No	0	Yes	4	- Not Applicable -		
MODULE (12 DIODE)	8656-1	T. I.	MIS17080/1-1	C-A	Yes	5	Yes	4	0.074		
MODULE CIRCUIT (+)		T. I.	MIS17080/1-1	C-A	No	0	Yes	4	0.12		
MODULE CIRCUIT (-)		T. I.	MIS17080/1-1	C-A	No	0	Yes	4	0.10		
RELAY CARD (+atgd)			11051275-9	C-A	No	0	Yes	6	0.094		
RELAY CARD (-atgd)			11051275-9	C-A	No	0	Yes	10	0.112		
S. C. R.	2N685	G. E.		C-G	Yes	1	Yes	4	1.4		
S. C. R.	2N1596	G. E.		C-G	Yes	3	Yes	2	0.94		
THYRISTOR (PNPN)	2N1602	T. I.		C-G	No	0	Yes	9	0.4		
THYRISTOR (PNPN)	2N1777A	T. I.	11040802-1	C-A	No	1	Yes	3	3.3		
THYRISTOR (PNPN)	2N1777A	T. I.	11040802-1	C-G	No	0	Yes	5	2.0	48.6°	0.0412
S. C. R.	2N2346	G. E.		C-A	Yes	1	Yes	2	2.7		
S. C. R.	2N2346	G. E.		C-G	Yes	1	Yes	3	3.7		
S. C. R.	SW3042	Transitron	MIS17224/1-1	C-G	Yes	3	Yes	4	0.165	1.01°	0.163

TABLE I (Continued)

SEMICONDUCTOR DAMAGE RESULTS FOR DIODES & SCR's (PERSHING).

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K^{-1} (WATT-SEC$^{1/2}$)	JUNCTION AREA (CM^2)X10^{-3}	K^{-1}/A $\left(\frac{\text{WATT-SEC}^{1/2}}{CM^2}\right)$ X10^3
TRANSISTOR (PNP)	2N329A		10630134	B-E	Yes	3	Yes	5	0.21		
TRANSISTOR (PNP)	2N329A			C-E	No	0	Yes	2	0.26		
TRANSISTOR (NPN)	2N335	G. E.	10630126-1	B-E	Yes	5	Yes	4	0.55	0.454°	1.21
TRANSISTOR (NPN)	2N336	G. E.		B-E	No	1	Yes	2	0.55	0.45°	1.21
TRANSISTOR (NPN)	2N336	G. E.		C-E	No	0	Yes	2	1.60		
TRANSISTOR (NPN)	2N336A	G. E.		B-E	No	0	Yes	6	0.34	0.454°	0.749
TRANSISTOR (NPN)	2N343	T. I.		B-E	No	0	Yes	7	0.047		
TRANSISTOR (PNP) +	2N375	Motorola		B-E	No	1	Yes	4	1.02		
TRANSISTOR (PNP) +	2N375	Motorola		C-E	Yes	3	Yes	3	0.195		
TRANSISTOR (NPN)	2N389	T. I.		B-E	No	1	No	1	38.4*	81.7	
TRANSISTOR (PNP)	2N495A	Sprague	10630119-1	B-E	Yes	2	Yes	8	0.70		
TRANSISTOR (NPN)	2N498	T. I.	10630123-1	B-E	No	2	Yes	3	0.80	5.42°	0.147
TRANSISTOR (PNP) +	2N526	G. E.		C-E	No	0	Yes	4	0.15		
TRANSISTOR (PNP) +	2N526	G. E.		B-E	No	0	Yes	5	0.39	2.27°	0.172
TRANSISTOR (NPN) +	2N576A	ETCO		B-E	No	0	Yes	5	0.023		
TRANSISTOR (PNP) +	2N618	Motorola		B-E	No	0	Yes	7	0.88		
TRANSISTOR (NPN)	2N657	T. I.		B-E	No	1	Yes	5	0.62	5.32°	0.116
TRANSISTOR (NPN)	2N657	T. I.		C-E	No	0	Yes	4	0.69		
TRANSISTOR (NPN)	2N657A	T. I.		B-E	No	1	Yes	4	1.07	5.32°	0.201

* ESTIMATED

° MANUFACTURER's QUOTE

\+ GERMANIUM DEVICE

TABLE II

SEMICONDUCTOR DAMAGE RESULTS FOR TRANSISTORS (PERSHING)

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K^1 (WATT-SEC$^{\frac{1}{2}}$)	JUNCTION AREA (CM^2)X10^{-3}	$K^1/A\left(\frac{\text{WATT-SEC}^{\frac{1}{2}}}{\text{CM}^2}\right)X10^3$
TRANSISTOR (NPN)	2N657A	T. I.		C-E	Yes	3	No	1	1.28		
TRANSISTOR (NPN)	2N657A	G. E.		C-E	Yes	2	Yes	3	1.07		
TRANSISTOR (NPN)	2N657A	G. E.		B-E	No	1	Yes	4	0.96	16.4°	0.0585
TRANSISTOR (NPN)	2N699	R. C. A.	10607051-1	B-E	Yes	3	Yes	5	0.25	0.777°	0.325
TRANSISTOR (NPN)	2N736	T. I.	10610121-1	B-E	No	0	Yes	3	0.10	0.081°	1.234
TRANSISTOR (NPN)	2N736	T. I.	10610121-1	C-E	Yes	2	Yes	4	0.042		
TRANSISTOR (NPN)	2N760A	National Semiconductor		B-E	No	0	Yes	5	0.034		
TRANSISTOR (PNP)	2N927	Solitron	10588790-1	B-E	No	0	Yes	4	0.10	0.38	0.262
TRANSISTOR (NPN)	2N930	T. I.	10588664-1	B-E	Yes	1	Yes	4	0.034	0.081°	0.421
TRANSISTOR (NPN)	2N930A	Motorola		B-E	No	0	Yes	3	0.02		
TRANSISTOR (NPN)	2N1016B	Westinghouse		B-E	No	0	Yes	3	1.6		
TRANSISTOR (NPN) +	2N1039			B-E	No	1	Yes	5	1.4	38.0	0.037
TRANSISTOR (PNP) +	2N1039			C-E	No	0	Yes	4	0.52		
TRANSISTOR (PNP) +	2N1099	Motorola		B-E	No	1	Yes	7	1.0		
TRANSISTOR (PNP) +	2N1115	ETCO		B-E	Yes	3	Yes	5	0.38		
TRANSISTOR (NPN)	2N1116A	Transitron		B-E	No	2	Yes	8	0.98	4.52°	0.217
TRANSISTOR (PNP)	2N1132	Transitron	10630132-1	B-E	Yes	2	Yes	5	0.23	1.14°	0.202
TRANSISTOR (PNP)	2N1132	Transitron	10630133-1	C-E	Yes	1	Yes	2	0.63		
TRANSISTOR (PNP)	2N1469			B-E	Yes	4	Yes	4	0.65		

TABLE II (Continued)

SEMICONDUCTOR DAMAGE RESULTS FOR TRANSISTORS (PERSHING)

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD FAILURE	FORWARD DEVICES TESTED (NO.)	REVERSE FAILURE	REVERSE DEVICES TESTED (NO.)	K^1 (WATT-SEC$^{1/2}$)	JUNCTION AREA (CM^2)X10^{-3}	K^1/A $\left(\frac{\text{WATT-SEC}^{1/2}}{CM^2}\right)X10^3$
TRANSISTOR (PNP)	2N1642	C. I.	10630133-1	B-E	No	0	Yes	8	0.13	0.12	1.08
TRANSISTOR (NPN)	2N1722	T. I.	10610120-3	B-E	No	0	No	3	54.5*	116.8°	
TRANSISTOR (NPN)	2N1893	T. I.		B-E	No	1	Yes	6	0.4	1.39°	0.288
TRANSISTOR (NPN)	2N1893	T. I.		C-E	No	0	Yes	3	0.4		
TRANSISTOR (NPN)	2N2222	T. I.	MIS17025/1-1	B-E	Yes	3	Yes	4	0.082	0.304°	0.271
TRANSISTOR (PNP)	2N2906	National Semiconductor		B-E	No	0	Yes	5	0.044		
UNIJUNCTION		T. I.	MIS17019/2-1	E-B_1	Yes	7	Yes	3	0.25	4.54°	0.055
DUAL XSISTOR (NPN)		Motorola	MIS17039/1-1	C-E	Yes	4	Yes	4	0.13		
DUAL XSISTOR (NPN)		Motorola	MIS17039/1-1	B-E	No	0	Yes	4	0.06		
TRANSISTOR (PNP)	SP2307	T. I.	MIS17181/1-1	C-E	No	1	No	1			
TRANSISTOR (PNP)	SP2307	T. I.	MIS17181/1-1	B-E	No	0	Yes	3	1.5	23.2°	0.0647
TRANSISTOR (NPN)		Motorola	MIS17186	B-E	Yes	3	Yes	4	0.033		
TRANSISTOR (NPN)		Motorola	MIS17186	C-E	No	0	Yes	2	0.052		
TRANSISTOR (PNP)		Motorola	MIS17240	B-E	No	0	Yes	4	0.071		
F. E. T. (N-channel)			MIS17331	G-S	No	0	Yes	5	0.103		
XSISTOR ASSBLY(NPN)		T. I.	MIS17409/1-1	C-E_2	Yes	4	No	1	5.0	25.9°	0.193
TRANSISTOR (NPN)		G. E.	10630127-1	B-E	No	0	Yes	3	0.12		
TRANSISTOR (NPN)		T. I.	10630127-1	B-E	No	0	Yes	5	0.059		

TABLE II (Continued)

SEMICONDUCTOR DAMAGE RESULTS FOR TRANSISTORS (PERSHING)

DEVICE DESCRIPTION	MANUFACTURER'S NOMENCLATURE	MANUFACTURER	PERSHING NO.	JUNCTION TESTED	FORWARD		REVERSE		K^1 (WATT-SEC$^{1/2}$)	JUNCTION AREA (CM^2)X10^{-3}	$K^1/A\left(\frac{\text{WATT-SEC}^{1/2}}{\text{CM}^2}\right)$X10^3
					FAILURE	DEVICES TESTED (NO.)	FAILURE	DEVICES TESTED (NO.)			
TRANSISTOR (NPN)	LN75497	R. C. A.	R227075497	B-E	No	1	Yes	4	1.9	65.7°	0.0289
TRANSISTOR (NPN)	LN75638	R. C. A.	R227075638	B-E	No	1	Yes	4	2.3	65.7°	0.035
I. C. (Gate Expander)	MC355G	Motorola	Inhouse	B-E	Yes	4	Yes	4	0.0062		
I.C. (Nand/NOR Gate)	SN7311	T. I.	Inhouse	B-E	Yes	4	Yes	4	0.082		
TRANSISTOR (NPN)	2N2222	Fairchild	Inhouse	B-E	Yes	3	Yes	7	.10	0.249	0.401
TRANSISTOR (NPN)	2N2222	Motorola	Inhouse	B-E	Yes	4	Yes	17	.10	0.273	0.366
TRANSISTOR (NPN)	2N2222	T. I.	Inhouse	B-E	Yes	10	Yes	17	.10	0.304°	0.333
TRANSISTOR (NPN)	2N2222	T. I.	Inhouse	C-E	Yes	4	Yes	3	.10		

TABLE II (Continued)

SEMICONDUCTOR DAMAGE RESULTS FOR TRANSISTORS (PERSHING)

SECTION 4.

NONSEMICONDUCTOR DEVICE TESTING

INTRODUCTION

Various electrical components (relays, capacitors, coils, etc.) were evaluated for damage vulnerability due to high voltage transients. In general, two areas were investigated for these nonsemiconductors: (1) device degradation resulting from the applied pulses (dielectric breakdown, changes in electrical responses or characteristics, etc.); and (2) internal arcing occurring during the pulse application. Virtually all of these device types proved to be "hard" for the maximum levels attainable with the BDM pulser.

Table I of this section summarizes the test results of the nonsemiconductor testing. This tabulation includes all the Pershing devices tested.

TEST PROCEDURE

Each device tested was multiple pulsed (10 times) across their terminals. In general, the pulser output was increased in 3 steps to its maximum output voltage (400 volts, 700 volts, and 1000 volts) for each tested component. The applied pulse width was 8 μ-seconds. Voltage and current photographs were taken for each of the selected pulse amplitudes and from these recordings the test data was reduced.

Degradation to any device was established by comparing various measurements taken by an impedance bridge before and after an applied pulse series. Using the bridge, the basic electrical characteristics could be measured for the various samples tested. Additionally, some components, such as motors and relays, had their rated potentials applied to them after the damage tests and observed for abnormal behavior during actual operation.

VACUUM TUBE DAMAGE TESTING

A cursory damage study was made to establish the vulnerability of vacuum tubes to high voltage transients. The complete experimental damage test results for tubes 6BC4, 6BX7, and 5876 is presented in Table II of this section. Although a brief study was conducted, the results did indicate that permanent damage to vacuum tube devices is possible with high voltage pulses.

TABLE I. NONSEMICONDUCTOR DEVICES (PERSHING)

Device Description	Pershing Number	Failure	Devices Tested
Brake Clutch	10640143	0	2
Capacitor	5910-060-1188	0	1
Capacitor	5910-669-3625	0	1
Capacitor	5910-814-6449	0	1
Capacitor	5910-823-1068	0	1
Capacitor	KF223KM*	0	1
Coil	5950-679-9539	0	2
Connector	10509676	0	1
Filter	MIS 17279/1-1	0	1
Filter	MIS 1749/6-1	0	1
Filter	11040553-1	0	1
Inductor	5950-845-6927	0	1
Motor	MIS 17103/1-3	0	1
Potentiometer	10607495-7	0	1
Potentiometer	106085l8-1	0	1
Potentiometer	106207495-11	0	1
Potentiometer	11040271-3	0	1
Relay	10607305	0	1
Relay	10630138	0	1
Relay	10630142	0	1
Relay	11040047-1	0	1
Relay	11040647	0°	2
Switch	1063009-1	0	1
Switch	1063009-3	0	1
Transformer	MIS 17088/2-1	0	1
Transformer	544-9715-002	0	1
Transformer	5950-856-6285	0	1
Transformer	11040499	0	1
Transformer	11040544-1	0	1
Transformer	11040545-1	0	1
Transformer	11040590-1	0	1

* Manufacturer's Number (WES CAP)
° Internal Arcing During Applied Pulses. Intermittent arcing at approximately 500 volts, constant arcover at approximately 700 volts.

TABLE II. VACUUM TUBE DAMAGE TEST RESULTS

TUBE	NUMBER TESTED	FAILURE	GRID-CATHODE VOLTAGE	PULSE WIDTH
6BX7[1]	3	0	+ 1KV	8μs
5876[2]	2	0	+ 1KV	8μs
6BC4[3]	3	2*	+ 1KV	8μs

Notes: * Transconductance (gm) decreased approximately 35% for both damaged devices.

[1] Medium - mu twin triode.

[2] Pencil type UHF high-mu triode.

[3] Medium - mu triode.

APPENDIX A

JUNCTION MODELING

THEORETICAL MODEL FOR JUNCTION FAILURE DUE TO TEMPERATURE

When a voltage pulse is applied to a semiconductor device in the reverse direction, the principal voltage drop is across the junction. An approximate thermal model for this situation is a plane source at the junction x = 0 in an infinite medium whose thermal conductivity and specific heat are functions of temperature. For silicon, the thermal conductivity is a sensitive function of temperature, e.g., from 1.56 watts/cm-°K at 300°K to 0.310 watts/cm-°K at 1000°K [24]; and since large temperature changes are anticipated, the change in thermal conductivity must be considered.

When the thermal conductivity and specific heat are functions of temperature, the general one-dimensional heat equation is [25]:

$$\frac{\partial}{\partial x}\left(\kappa\frac{\partial T}{\partial x}\right)-\rho C_p\frac{\partial T}{\partial t}=0 \tag{1}$$

where κ = thermal conductivity [watt/cm-°K]; ρ = density [grams/cm^3]; C_p = specific heat [joules/gm-°K]; t = time [sec]; T = temperature [°K]; and x = distance [cm].

By a change of variables,

$$\theta=\int_o^T\frac{\kappa}{\kappa_o}\,dT, \tag{2}$$

equation can be written as [25].

$$\frac{\partial^2\theta}{\partial x^2}-\frac{1}{\partial(\theta)}\frac{\partial\theta}{\partial t}=0 \tag{3}$$

This equation is similar to the familiar heat equation except that α is a variable which depends on θ. For the semiconductor failure problem, actual junction geometries vary from device to device, and the exact junction mechanisms are not necessarily consistant. Because of these uncertainties,

certain simplifying assumptions are justified. Therefore, temperature variations for the semiconductor failure model will be described by

$$\frac{\partial^2 T}{\partial x^2} - \frac{1}{\alpha}\frac{\partial T}{\partial t} = 0 \tag{4}$$

where α is a constant. Corrections for possible over-simplifying assumptions can be made by using an 'effective' or time-weighted average of κ over the temperature range of interest. The weighting will be done by considering the time interval in each temperature interval considering the change in temperature is given by $\Delta T = At^{1/2}$ (which we will find is the form of our solution).

The solution of equation (4) for an infinite medium with an instantaneous plane source of strength Q, at t = 0, parallel to the plane x = 0 and passing through x' with zero initial temperature is given by

$$T = \frac{Q}{(4\alpha\pi t)^{1/2}}\, e^{-(x-x')^2/4\alpha t}, \tag{5}$$

where the heat liberated per unit area is QoC_p. For a rectangular heat source, of duration t, $Q = Q(t') = q$ = constant, and the temperature rise is

$$T = \frac{q}{(4\pi\alpha)^{1/2}} \int_o^t \frac{e^{\frac{-(x-x')^2}{4\alpha(t-t')}}}{(t-t')^{1/2}}\, dt' . \tag{6}$$

Performing the integration,

$$T = q\left(\frac{t}{\pi\alpha}\right)^{1/2} e^{\frac{-(x-x')^2}{4\alpha t}} - \frac{q|x-x'|}{2\alpha}\, \operatorname{erfc}\left(\frac{|x-x'|}{2\sqrt{\alpha t}}\right) \tag{7}$$

Making the substitution x = 0 and x' = 0, then equation (7) fits the

requirements of the thermal model for semiconductor heating at the junction, and

$$T(0) = q\left(\frac{t}{\pi\alpha}\right)^{1/2} \tag{8}$$

represents the junction temperature increase caused by a pulse of width t which heats the junction at a rate q. The heat per unit area per unit time is given by the power per unit area divided by the specific heat and the density, i.e.,

$$q = \frac{P}{A}\ \frac{1}{\rho C_p}\ . \tag{9}$$

If the initial junction temperature is T_i, then $T \rightarrow \Delta T = [T-T_i]$, and equation (8) becomes

$$[T-T_i] = \frac{P}{A}\ \frac{t^{1/2}}{\sqrt{\pi\kappa\rho C_p}}\ . \tag{10}$$

Experimental guidelines are obtained from equation (10) if temperature extremes, within which junction failure is deemed likely to occur, can be estimated. Defining T_m to be the junction failure temperature, the power per unit area as a function of time is given by

$$\frac{P}{A} = \sqrt{\pi\kappa\rho C_p}\ [T_m-T_i]\ t^{-1/2} \tag{11}$$

Three cases are of interest. The constants for these cases are:

ρ = 2.33 gm/cm^3, C_p = 0.7566 joules/gm-°K, T_i = 25°C, and κ (effective) = 0.526 watts/cm-°K (Case I), and κ (effective) = 0.306 watts/cm-°K (Cases II and III). (For time in microseconds, P/A is given in kilowatts/cm^2.)

Case I - Heating from room temperature 25°C (~300°K) to a temperature of 675°C (948°K). Equation (11) is then:

$$P/A = 1109.4\ t^{-1/2}$$

Case II - Heating from room temperature 25°C (~300°K) to the melting temperature of silicon 1415°C (1688°K), (excluding phase change energy). Equation (11) is then:

$$P/A = 1809.7\ t^{-1/2}$$

Case III - Same as Case II except that the current is assumed to pass through local hot spots and the power is dissipated in one-tenth of the total area. The failure temperature is the hot spot temperature.

Semiconductor failure levels should fall within these limits, and plots for these three cases should give an indication of the reliability of experimental data.

As previously mentioned an effective value of thermal conductivity was used in the calculations above. The thermal conductivity of silicon is neither a constant nor a linear junction of temperature as indicated in Fig. A-1. Values of the thermal conductivity κ for 100°K intervals are given in Table A-1. It should be noted that the first and last values are given for 50°K intervals. Since $\Delta T = C_1\sqrt{t}$, setting $\Delta T = 100$ for a full interval for a unit time will give $C_1 = 100$. Setting $\Delta T = 50$ for the first step will then given $t = 1/4$. The time differential Δt_i represents a relative time increment between intervals weighted with respect to the time during which power is delivered to the junction, whereas t_i represents the relative time with reference to the total pulse duration. The value of κ_i is the thermal conductivity at the midpoint of the intervals and represents an average value in the temperature range indicated.

The table values given can be used to determine the effective thermal conductivity κ_{eff} in an arbitrary temperature range according to the formula:

$$\kappa_{eff} = \frac{\sum_i \Delta t_i \kappa_i}{\sum_i \Delta t_i} \qquad (12)$$

EXAMPLE 1. Determine the effective thermal conductivity for silicon in the temperature range from room temperature (300°K) to a terminal temperature of 950°K.

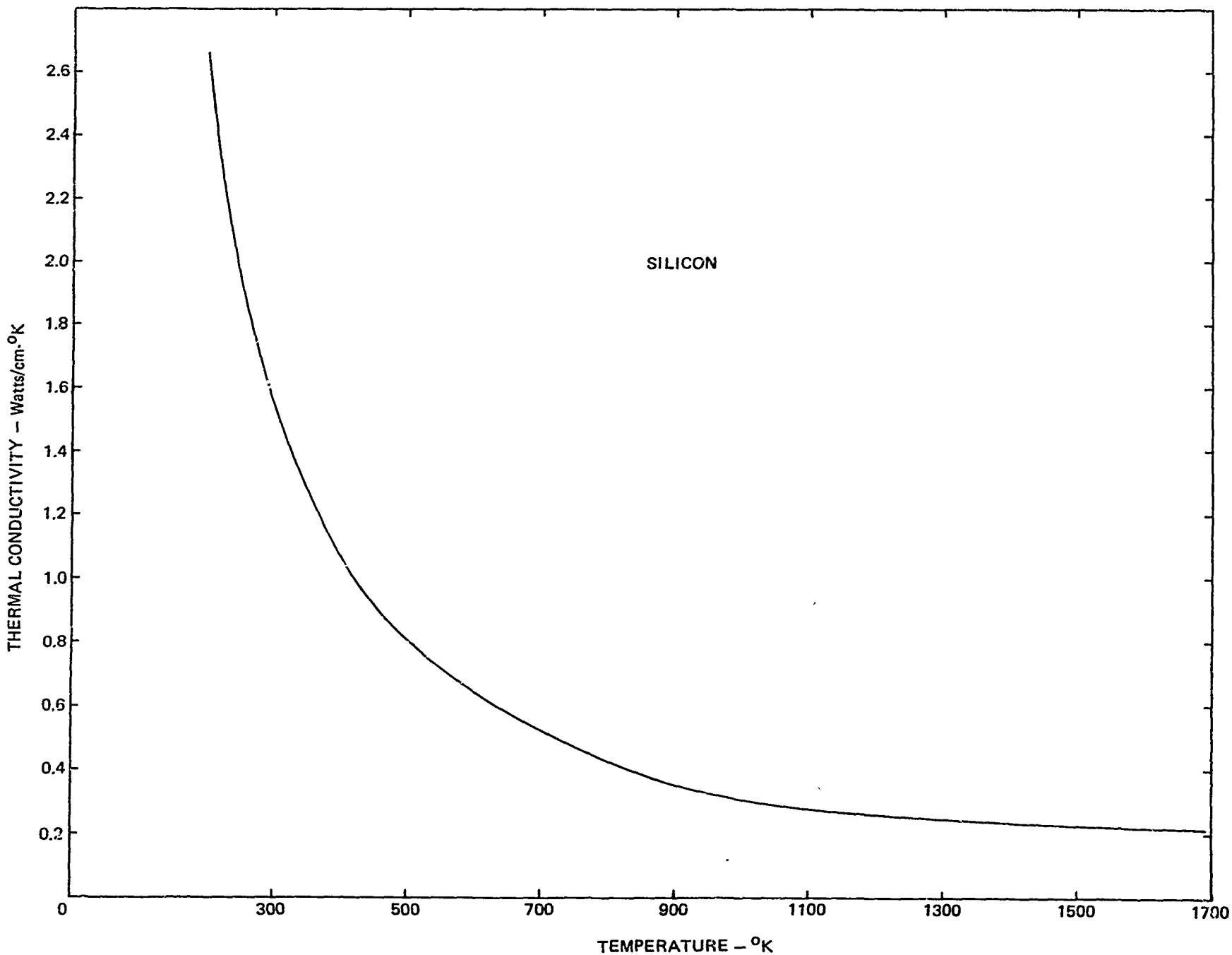


Figure A-1. Thermal Conductivity of Silicon

Table A-1 Values of Thermal Conductivity for Silicon

T(°K)	ΔT_i	t_i	Δt_i	κ_i	$\Delta t_i \kappa_i$
300-350	$\frac{1}{2} C_1$	1/4	1/4	1.360	0.34
350-450	$\frac{3}{2} C_1$	9/4	2	1.050	2.10
450-550	$\frac{5}{2} C_1$	25/4	4	0.800	3.20
550-650	$\frac{7}{2} C_1$	49/4	6	0.640	3.84
650-750	$\frac{9}{2} C_1$	81/4	8	0.520	4.16
750-850	$\frac{11}{2} C_1$	121/4	10	0.430	4.20
850-950	$\frac{13}{2} C_1$	169/4	12	0.356	4.27
950-1050	$\frac{15}{2} C_1$	225/4	14	0.310	4.34
1050-1150	$\frac{17}{2} C_1$	289/4	16	0.280	4.48
1150-1250	$\frac{19}{2} C_1$	361/4	18	0.261	4.70
1250-1350	$\frac{21}{2} C_1$	441/4	20	0.248	4.96
1350-1450	$\frac{23}{2} C_1$	529/4	22	0.237	5.21
1450-1550	$\frac{25}{2} C_1$	625/4	24	0.227	5.45
1550-1650	$\frac{27}{2} C_1$	729/4	26	0.219	5.69
1650-1700	$\frac{28}{2} C_1$	784/4	13-3/4	0.216	2.97

SOLUTION:

Sum of column $\Delta t_i \kappa_i$ from 300°K to 950°K = 22.21

Sum of column Δt_i from 300°K to 950°K = 42.25

$$\kappa_{eff} = \frac{22.21}{42.25} = 0.526 \text{ w/cm-°K.}$$

EXAMPLE 2. Determine the effective thermal conductivity of silicon in the temperature range from room temperature (300°K) to 1,700°K (melting point of silicon).

SOLUTION:

Sum of column $\Delta t_i \kappa_i$ from 300°K to 1, 700°K = 60.01

Sum of column Δt_i from 300°K to 1,700°K = 196

$$\kappa_{eff} = \frac{60.01}{196} = 0.306 \text{ w/cm-°K.}$$

The thermal conductivity versus temperature for germanium is given in Fig. A-2. A table of values for germanium similar to that discussed for silicon is given in Table A-2. The effective value for the thermal conductivity of germanium for the temperature interval 300°K to 1210°K (melting point of germanium) was calculated to be 0.202 watts/cm-°K. Solving equation 11 for germanium using the constants ρ = 5.33 gm/cm^3, C_p = 0.3093 joules/gm-°K, T_i = 25°C, T_m = 937°C, and κ effective = 0.202 watts/cm-°K, the power per unit area for failure is given by

$$P/A = 933\ t^{-1/2}.$$

Table A-2 Values of Thermal Conductivity for Germanium

T(°K)	ΔT	t	Δt	κ	(Δt)κ
300					
350	1/2 C_1	1/4	1/4	0.55	0.138
450	3/2 C_1	9/4	2	0.44	.88
550	5/2 C_1	25/4	4	0.34	1.36
650	7/2 C_1	49/4	6	0.27	1.62
750	9/2 C_1	81/4	8	0.22	1.76
850	11/2 C_1	121/4	10	0.19	1.90
950	13/2 C_1	169/4	12	0.18	2.16
1050	15/2 C_1	225/4	14	0.17	2.38
1150	17/2 C_1	289/4	16	0.17	2.72
1210	18.2/2 C_1	331.2/4	10.55	0.17	1.793

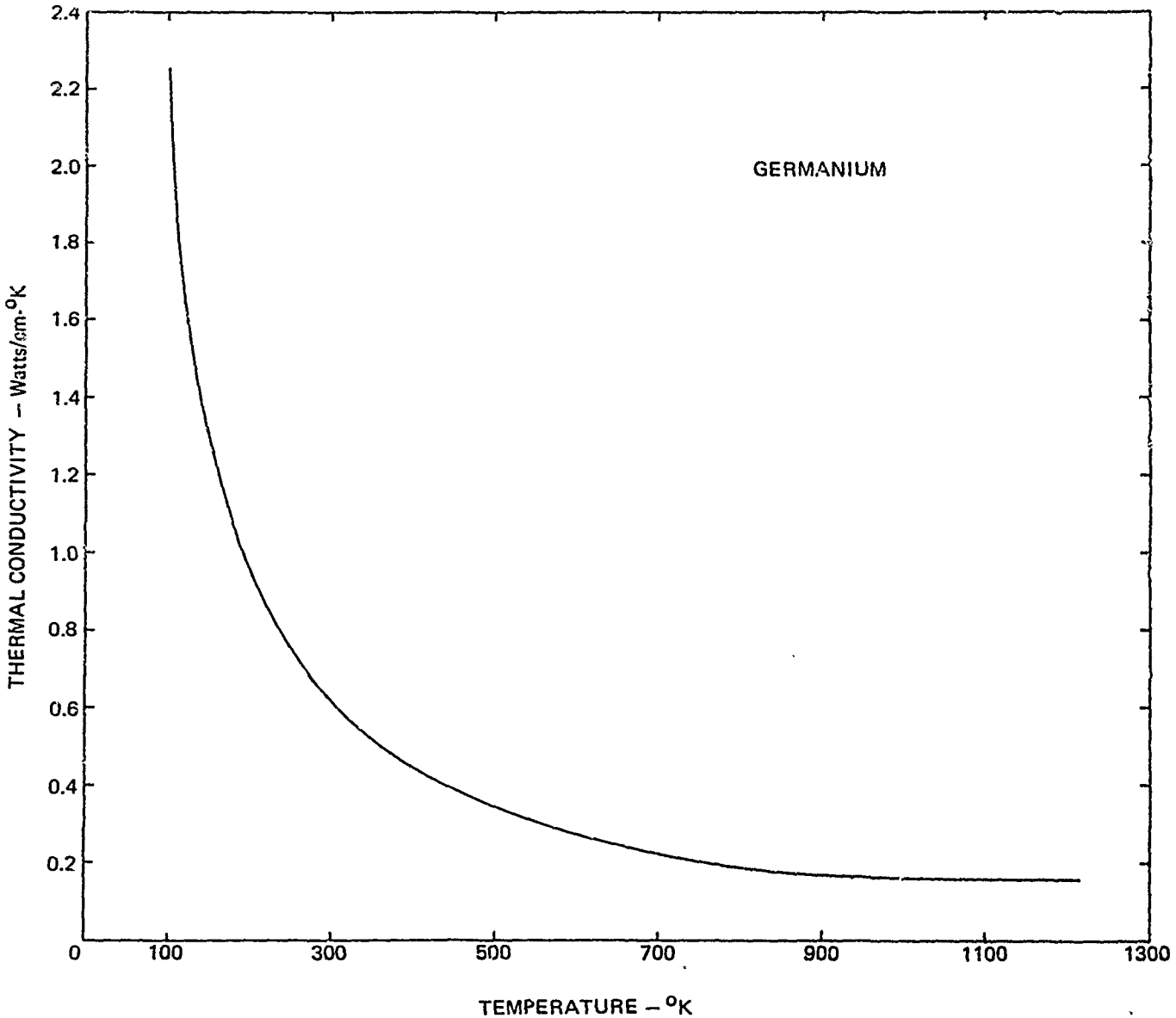


Figure A-2. Thermal Conductivity of Germanium

Theoretical Voltage and Current Calculations

1. Reverse Polarity Calculations

The calculation of the breakdown voltage in the reverse direction has been adequately described for certain conditions. In the reverse direction, two different microscopic mechanisms occur:

1. Avalanche breakdown and
2. Zener breakdown

The normal VI characteristic for a p-n diode, $I = I_o[e^{qV/kT}-1]$ gives the correct current in the reverse direction [V negative] and then $I = -I_o$ when the absolute magnitude of -V is much much greater than kT/q until some maximum reverse voltage V_B is reached. Then the equation no longer applies and the reverse current increases very rapidly. The physical phenomenon which causes the reverse breakdown is called the avalanche effect. It is a carrier multiplication effect which occurs in the p-n junction when a sufficiently large voltage is applied in the reverse direction. It is a non-destructive mechanism in itself. The reverse current characteristic is microscopically described as follows. As the holes [or electrons] which constitute the staturation current I_o move through the junction region, they gain energy from the electric field and then give it up when they collide with the lattice. For smaller electric field intensities, all the energy is given up to the lattice with each collision with the lattice and the hole continues through the junction with no increase in current. As the electric field intensity increases, the hole gains more energy per mean free path length and due to quantum-mechanical considerations, does not give up all of its energy with each collision. Hence, the hole keeps gaining energy with each mean free path until it has sufficient energy to ionize the lattice upon collision, thereby, releasing more free hole-electron pairs. This multiplicative action continues and the avalanche current is produced.

If the current is limited by circuit resistance or by time durations, there is no damage to the device. The avalanche breakdown is the normal breakdown mechanism in junctions with light doping and wide junction regions.

The Zener breakdown is the field-induced direct transition of carriers from the valence band to the conduction band. This breakdown (essentially field emission) occurs when the electric field strength reaches values of approximately 10^6 volts/cm or higher. As the doping level increases, the mean free path length decreases so with narrow junction widths, a particle cannot gain sufficient energy to cause ionizing collisions, but the field is strong enough to cause direct transition. Thus, again the current sharply increases from its saturation level due to the Zener breakdown which again is non-destructive if the current is limited. (This same effect is the one that changes the shape of the forward current characteristic and gives a negative resistance region for tunnel diodes.)

Again, there has been considerable theoretical work done in calculating the reverse breakdown voltage. These calculations agree well with experimental evidence if the physical parameters of the junction are known.

Although reverse breakdown voltages can be theoretically calculated it does not appear to be worthwhile to do this for the study of failure levels. In order to make accurate calculations the physical parameters of the junction need to be accurately known. The needed information is often not readily available from the manufacturer. The reverse breakdown voltage for the device can be easily measured experimentally. As long as the reverse current is limited during the test there is no damage to the device. The breakdown voltage determined experimentally is more accurate and gives an exact breakdown level for the particular device to be tested later for failure level.

2. Forward Polarity Calculations

The calculation of current and junction voltages for forward conduction has been quite well established for the lower current levels. The current calculated from $I = Io[e^{qV/kT}-1]$ matches closely with experimental values. For

large currents these relationships are no longer valid. At large currents there is an appreciable IR voltage drop across the bulk resistance of the diode. Kano and Reich [26] have discussed a model for calculation of transient parameters when the forward current levels are quite high. However, their model is based on a step impulse of current rather than voltage. Their results indicate that the equation above is still valid for quite large currents provided that the voltage value used in the equation is the actual voltage across the junction rather than the terminal voltage. Thus the current is given by

$$I = Io\ [e^{qV_j/kT} - 1],$$

where $V_{junction} = V_{terminal} - V_{bulk\ resistance}$.

A plot of the V-I characteristics are as shown in Figure A-1.

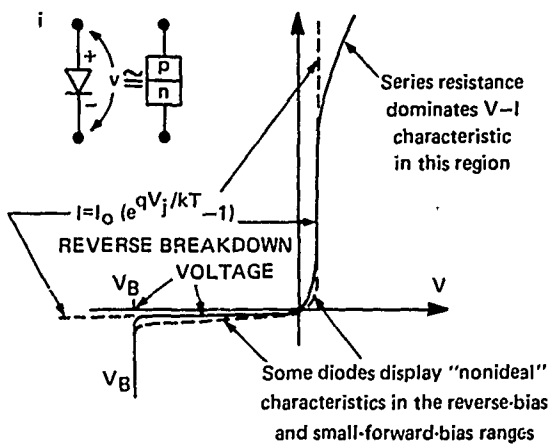


Figure A-1

In order to make temperature rise calculations, the voltage and the current across the junction must be known.

Since the current rises as an exponential function of the junction voltage, this voltage can be considered to be a constant in calculating the power dissipated in the junction. Attention is now given to the temperature calculations in order to determine the failure levels. The power can be calculated from $P = V_j Io\ e^{qV_j/kT}$ for high current levels. To perform a more accurate failure calculation, the heat dissipated in the bulk resistance must be considered since it can be appreciable at high current levels.

APPENDIX B

TRANSISTOR BASE-EMITTER JUNCTION PROTECTION AGAINST HIGH VOLTAGE TRANSIENTS BY THE USE OF DIODES

I. GENERAL

Previous work performed by the laboratory indicates that the transistor junction most susceptable to high voltage transients is the base-emitter. This is primarily because of its low zener voltage and small cross-sectional area.

This report describes several means of protecting this junction against damage with the use of high peak inverse voltage diodes and zener diodes. The advantages and disadvantages of these protection devices will also be discussed.

Since the laboratory has obtained a good collection of data on the 2N2222 transistor, this device was used in the experimental test conducted for this study.

II. 2N2222 CHARACTERISTICS AND DAMAGE LEVELS

A. Characteristics

The base-emitter junction of a typical 2N2222 is rated at a reverse bias breakdown voltage (V_{BEO}) equal to 6 volts DC. The mean value of the devices tested was 7.8 volts DC with a spread being from 7.0 to 8.8 volts DC. The emitter cut-off current which flows from the emitter to the base is rated at a maximum value of 10 nanoamperes DC with a 3 volt DC reverse bias present on the base emitter junction. Beyond the zener knee, the dynamic resistance of the junction is 7.5 ohms about 200 milliamperes.

In the forward direction, the junction exhibits a resistance of 2.3 ohms at a forward current of 0.5 amps DC and 1.56 ohms at 1 ampere. The dynamic resistance in both cases is approximately 0.8 ohms.

B. Damage Levels

Typical failure points for the 2N2222 in the reverse and forward direction are shown in Figure 1. Each point represents a total loss of the base-emitter diode characteristic. No attempt is made here to indicate

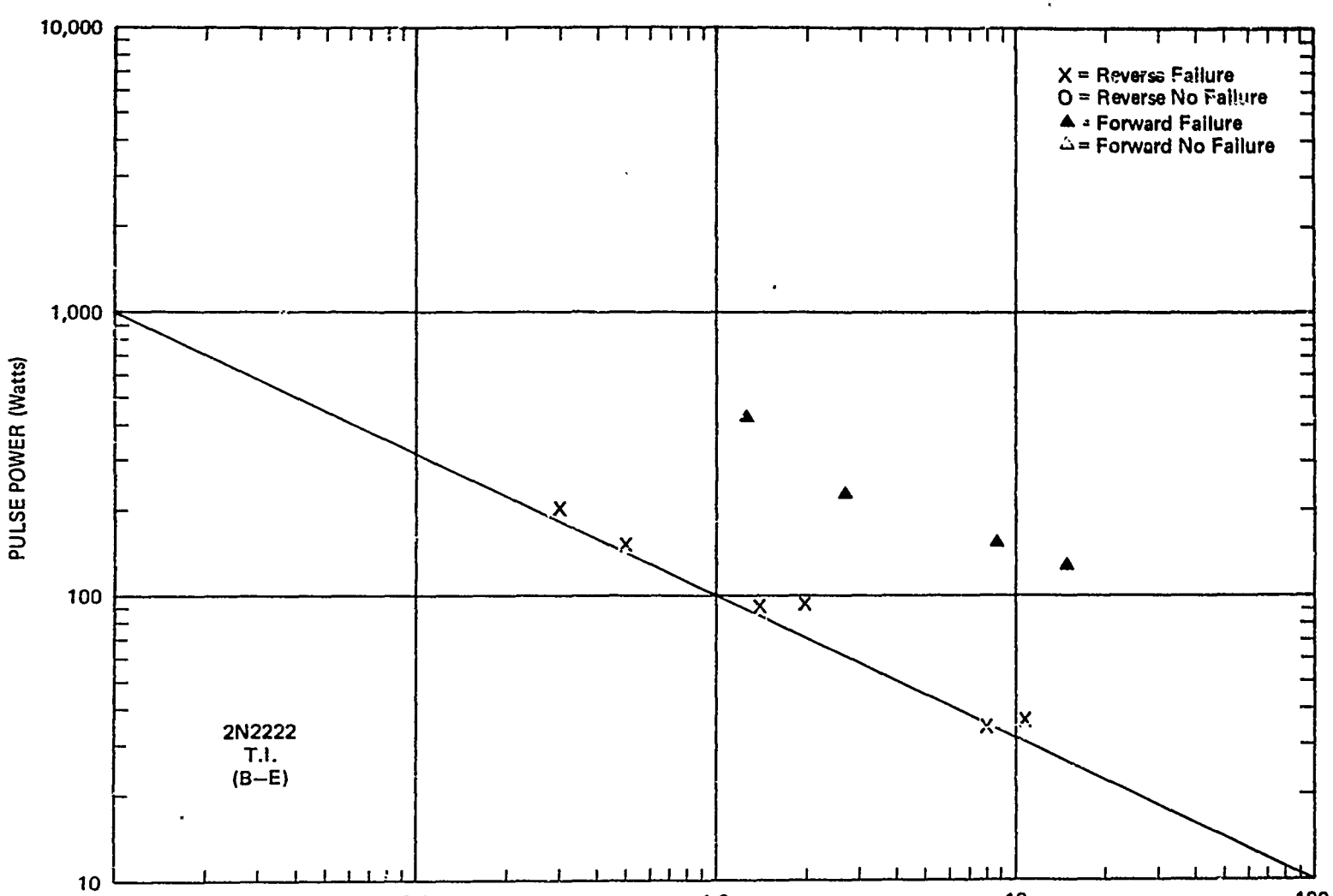

10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
T.I.
(B–E)

Figure 1

degradation in zener potential or reverse leakage current. The points indicated are representative of the actual peak junction dissipation in the reverse direction of a single high voltage transient applied to the junction. Junction current and voltage data was obtained with a fast trace recording camera.

III. PROTECTION AGAINST REVERSE TRANSIENTS

A. Series Diode

The base-emitter junction is capable of conducting large amounts of peak power because of its very low zener potential (6-10 volts). The zener potential can be increased without degrading the normal operation of a circuit by inserting a high peak inverse voltage diode in series with the emitter of the transistor (see Figure 2A). This combination will not draw reverse current until the zener potential of the additional diode is exceeded.

A test was run with a 1N645 diode (which has a rated PIV equal to 275 volts DC) in series with the emitter of a 2N2222. Where the 2N2222 usually conducts 25 amperes with an applied 1KV pulse, the current drawn for the combination was less than 80 milliamperes. The junction was not damaged by conduction times as long as one microsecond.

The advantage of this technique is that high peak inverse voltage diodes have very low capacitance, high back resistance and a relatively low forward drop so as not to degrade the circuit's normal performance.

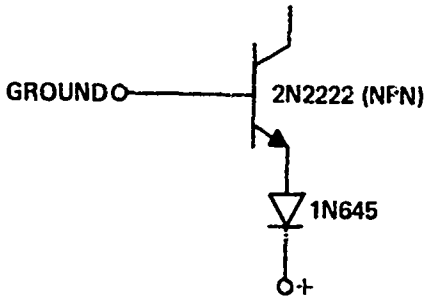
The major disadvantage, of course, is that the diode does not offer any forward transient protection.

B. Shunt Zener Diode

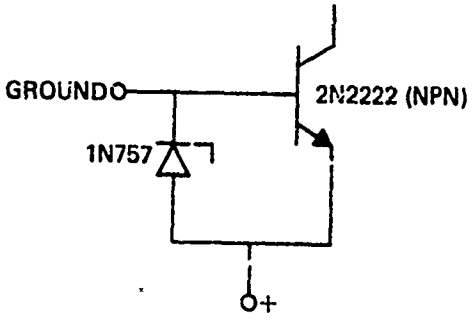
Another method of reducing the dissipation of the base-emitter junction of the transistor is to shunt the current around the junction and dissipate the power in a stronger device (see Figure 2B).

The zener diode will protect the junction in the reverse transient case by conducting in its normal forward direction. Care must be used to be sure that a temperature compensated zener is not used as this would require a very high voltage to overcome the PIV of the compensating diode.

A. SERIES DIODE (REVERSE PROTECTION)



B. SHUNT DIODE (REVERSE PROTECTION)



C. SHUNT DIODE WITH SERIES R_B (FORWARD PROTECTION)

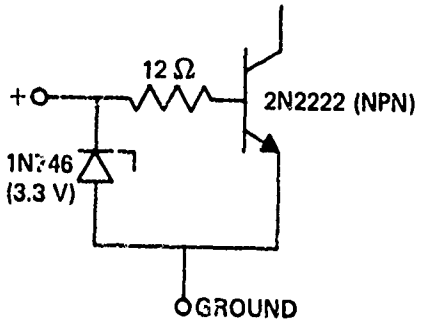


Figure 2. Protection Circuits Against Transients.

For the forward transient case, the base-emitter junction would conduct before the zener even with a low voltage zener. High voltage transients would cause the zener diode to avalanche but not until the base-emitter junction had already heavily conducted large amounts of current, damaging the junction.

Tests conducted show that indeed the shunt zener did protect against reverse damage transients but failed to protect against the forward transients.

Another disadvantage of the shunt diode protection circuit is the large amount of capacitance that the diode presents to the driving source. A typical value of 1 volt reverse bias capacitance for a low voltage zener is on the order of 500 picofarads. This additional capacitance, depending upon the applications, may be highly degrading upon the operation of the circuit.

IV. PROTECTION AGAINST FORWARD TRANSIENTS

A. Shunt Zener Diode with Series Base Resistance

The reason the shunt zener diode failed to protect the base-emitter junction against forward transients is because of the zener impedance being higher than the base-emitter saturation resistance. Increasing the saturation resistance of the base-emitter junction by inserting a small resistor in series with the base will cause the zener to handle the majority of the current. The small resistor will not effectively degrade the normal performance of the circuit (see Figure 2C).

Data obtained from experimental tests of this configuration indicated that with a 12 ohm base series resistance the 3.3 volt zener diode conducted approximately 32 amperes while the base-emitter junction conducted only 0.5 amperes with a 1 kilovolt pulse applied to the configuration in the forward direction. No damage was done to either of the semiconductor deivces.

Removal of the zener diode and testing with only the series base resistance indicated the expected failure.

The shunt zener diode in this configuration has the same disadvantages mentioned previously in Section III-B. The large shunt capacitance may be detrimental to the normal operation of high-speed circuitry.

V. OTHER PROTECTIVE DIODES INVESTIGATED

Thyristors, specifically four-layer trigger diodes and switching tunnel diodes were briefly investigated as possible protective devices because of their high switching speed. A review of the possible application of these devices indicated that the limited dissipation capabilities and self susceptability of these devices to transients of this type prohibit their use. The limited number of devices which have higher power dissipation capabilities do not appear to be any harder.

M, Inc. Paso S	Device 2N2222 Type NPN XSISTOR MIS PPN	MFG T.I. V_{CBO} v. V_{CEO} v. V_{BEO} v.	PIV v. I A. @p ms.
V_{FX} v. V_{RO} v. V_{GT} v. I_H ma.	H_{FE} @V_{CE} 10 v. @I_C 10 ma.	Test Junction B-E By: L. Marzitelli On: 2/9/68	

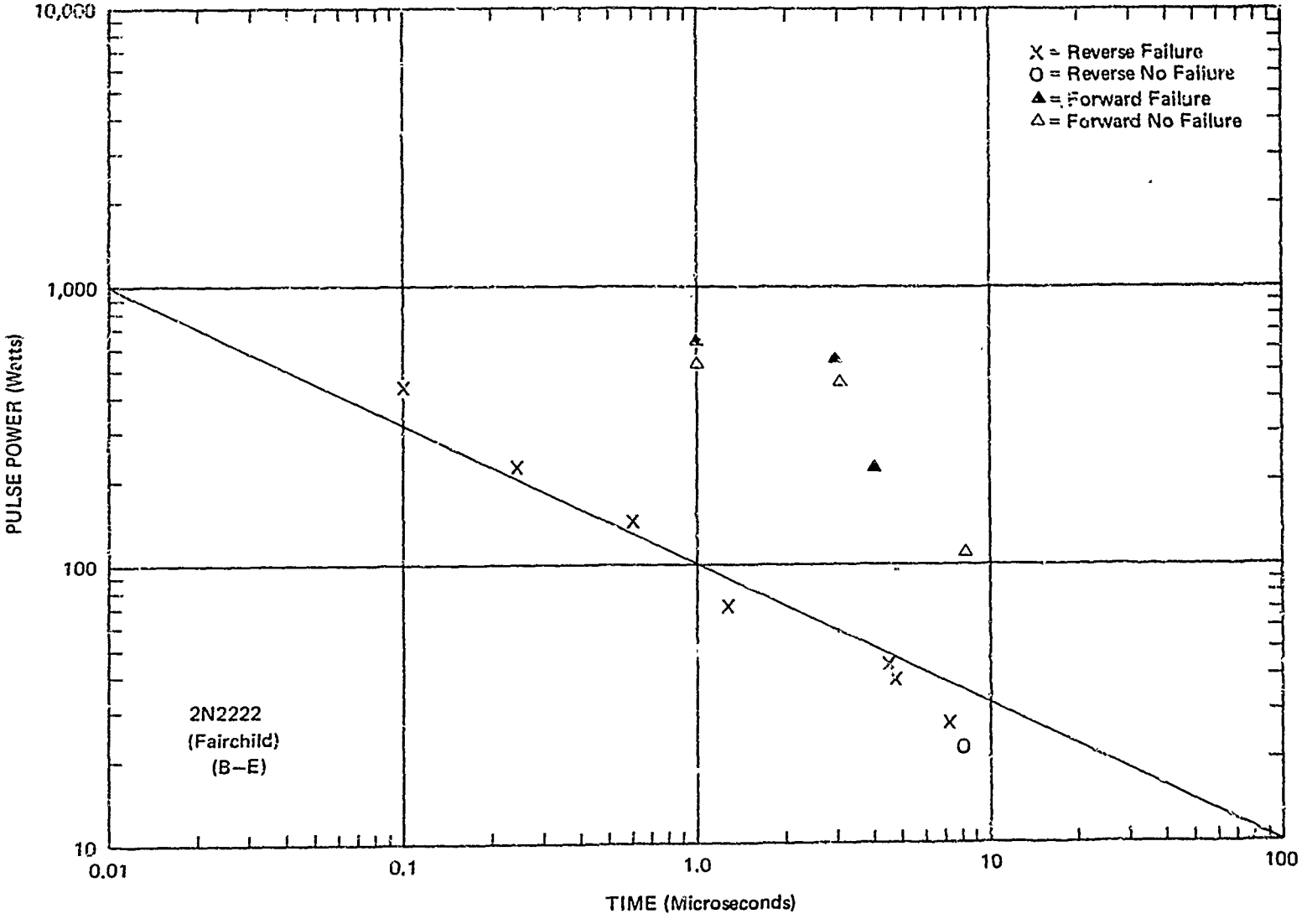
vice .	Data Pt.	T_D (μs)	T_{DOC} (μs)	V_p (V)	I_p (A)	$V_p \times I_p$ (Watts)	Energy (μ Joules)	V_{oc} (V)	V_{ZB} (V) @50μa	V_{ZA} (V) @50μa	H_{FE} (BEF)	H_{FE} (AFT)	Polarity (Emitter to Base)	Failure	Remarks
	NOTE:	for following tests, 1N645 is reverse biased and is in the emitter circuit.													
72	1	.9	1	400				400	7.2	7.2	115	115	REV	NO	1N645 V_z 950v@50μa
	2	.9	1	630				630		7.2		115	REV	NO	
	3	1	1	800				800		7.2		115	REV	NO	
	4	1	1	900				900		7.2		115	REV	NO	
	5	1	1	1KV	.06	60	60	1KV		7.2		115	REV	NO	1N645 shows no degradation
	6	1	1	1KV	.08	80	80	1KV		7.2		115	REV	NO	XSISTOR shows no damage
	NOTE:	for following tests, zener diodes, 1N757, is between B & E; diode's anode is tied to emitter													
	7	1	1	45	14	630	630	400		7.2		115	REV	NO	1N757 V_z is 9.6v
	8	1	1	60	22	1320	1320	600		7.2		115	REV	NO	
	9	1	1	70	28	1960	1960	800		7.2		115	REV	NO	
	10	1	1	85	34	2890	2890	1KV		7.2		115	REV	NO	XSISTORshow no degradation
	11	2.4	10	16	26	416	999	800		0		0	FWD	YES	1N757 still good(V_z=9.6
	NOTE:	for following tests, zener diode, 1N746, in series W/12Ω, is between B & E; anode of diode is tied													
		to emitter of transistor. Pulsing between emitter and diode's cathode.													
72	1	4.2	10	9	24*	4.5"	18.9'	800	7.0	7.0	149	149	FWD	NO	1N796 V_z is 1.6V@50μa
	2	5.6	>16	10	32*	5.0"	18'	1KV		7.0		149	FWD	NO	*I thru XSISTOR is 0.5 amps
	NOTE:	for following tests, 12Ω is in series with the Base lead. Zener is removed.													
	3	6.4	10	280*	16	240"	1535'	1KV	7.0	0	149	0	FWD	YES	*V across XSISTOR is 15v(280v is across 12Ω +XSISTOR)
	NOTE:	' actual energy dissipated in device.													
		" actual power dissipated in device.													

APPENDIX C

THRESHOLD POWER FAILURE CURVES FOR DEVICES 2N2222, MC267G, MC355G, AND SN7311.

Concurrent with the Pershing semiconductor damage study, additional devices were tested as part of BDM "in-house" study program. Extensive damage testing of the 2N2222 silicon NPN transistor was conducted and the results from this device were used to assist in the validation of the thermal failure model. Also, three integrated circuits, MC267G, MC355G, and SN7311, were studied. The damage information from the three I. C.'s served as a comparison to that data gotten from the discrete transistors and diodes tested for the overall program.

The following pages of this appendix contain the threshold power failure curves for the in-house study devices. Note that for the 2N2222 transistor, curves are also presented for conditions where the case temperature was elevated before pulse application to the B-E junction. The complete results of all these tests are included in Tables I and II of Section 3.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0.01
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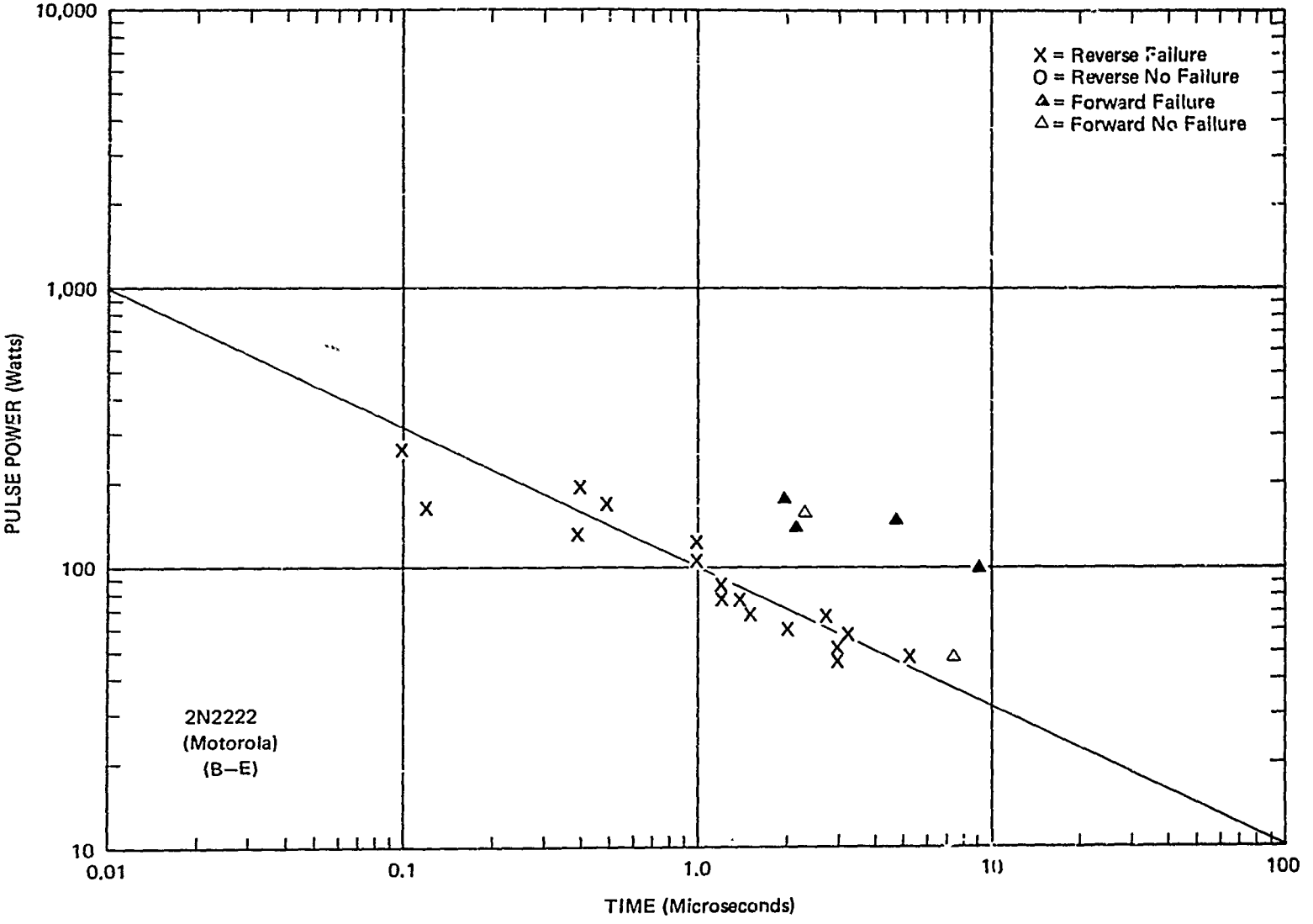
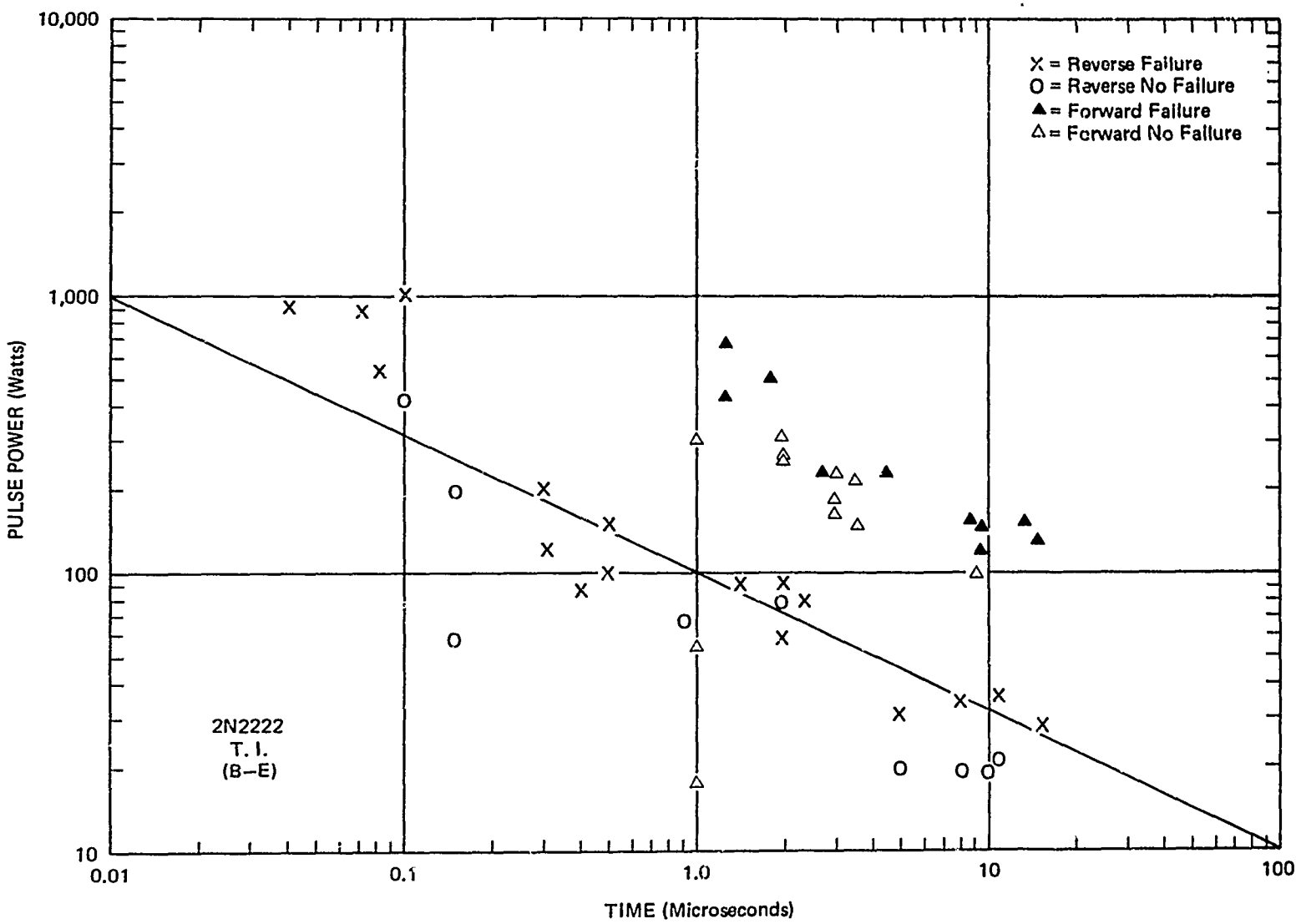
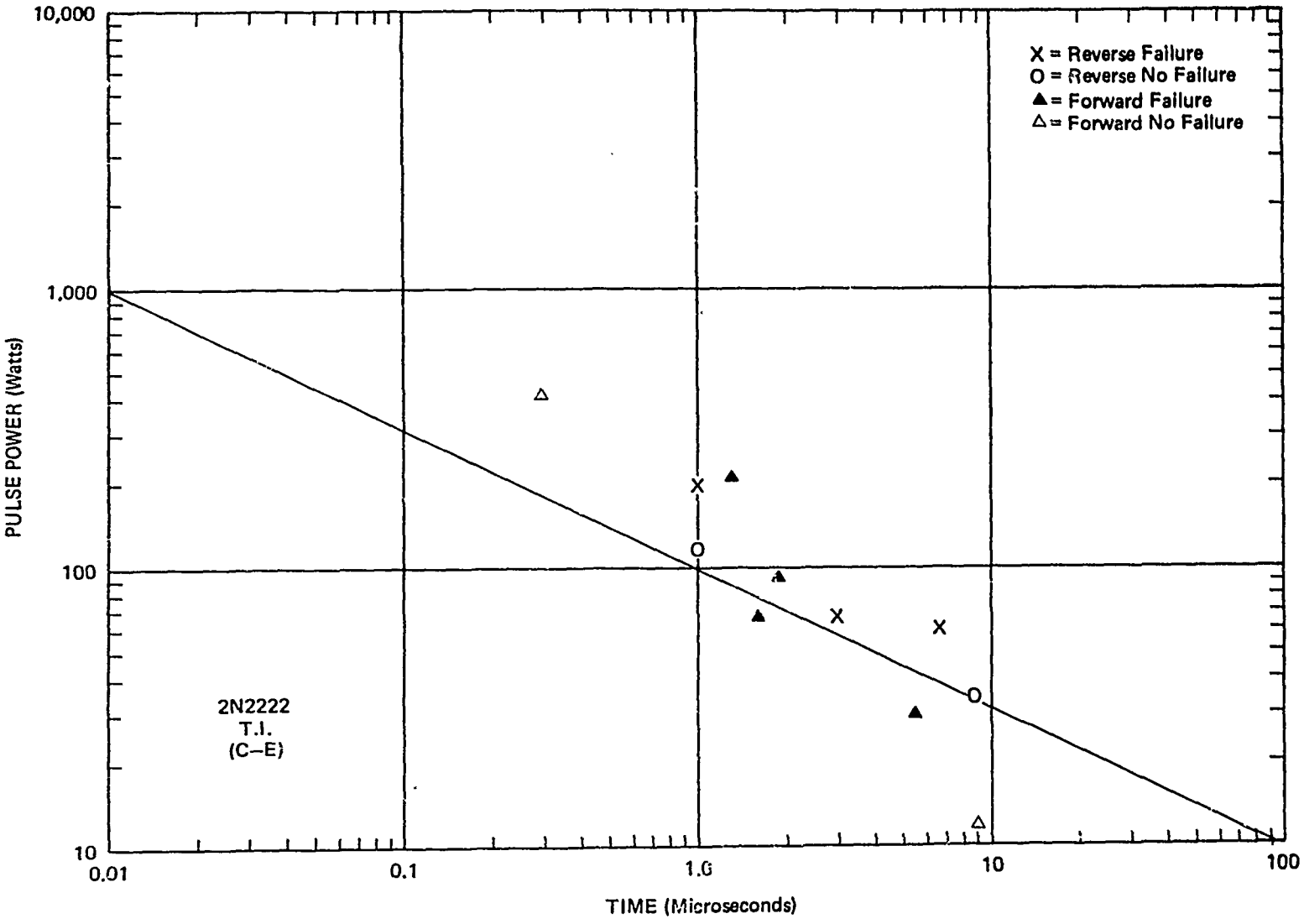
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
(Fairchild)
(B–E)


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
(Motorola)
(B–E)


10,000
1,000
100
10
PULSE POWER (Watts)
0.01
0.1
1.0
10
100
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
T. I.
(B–E)


10,000
1,000
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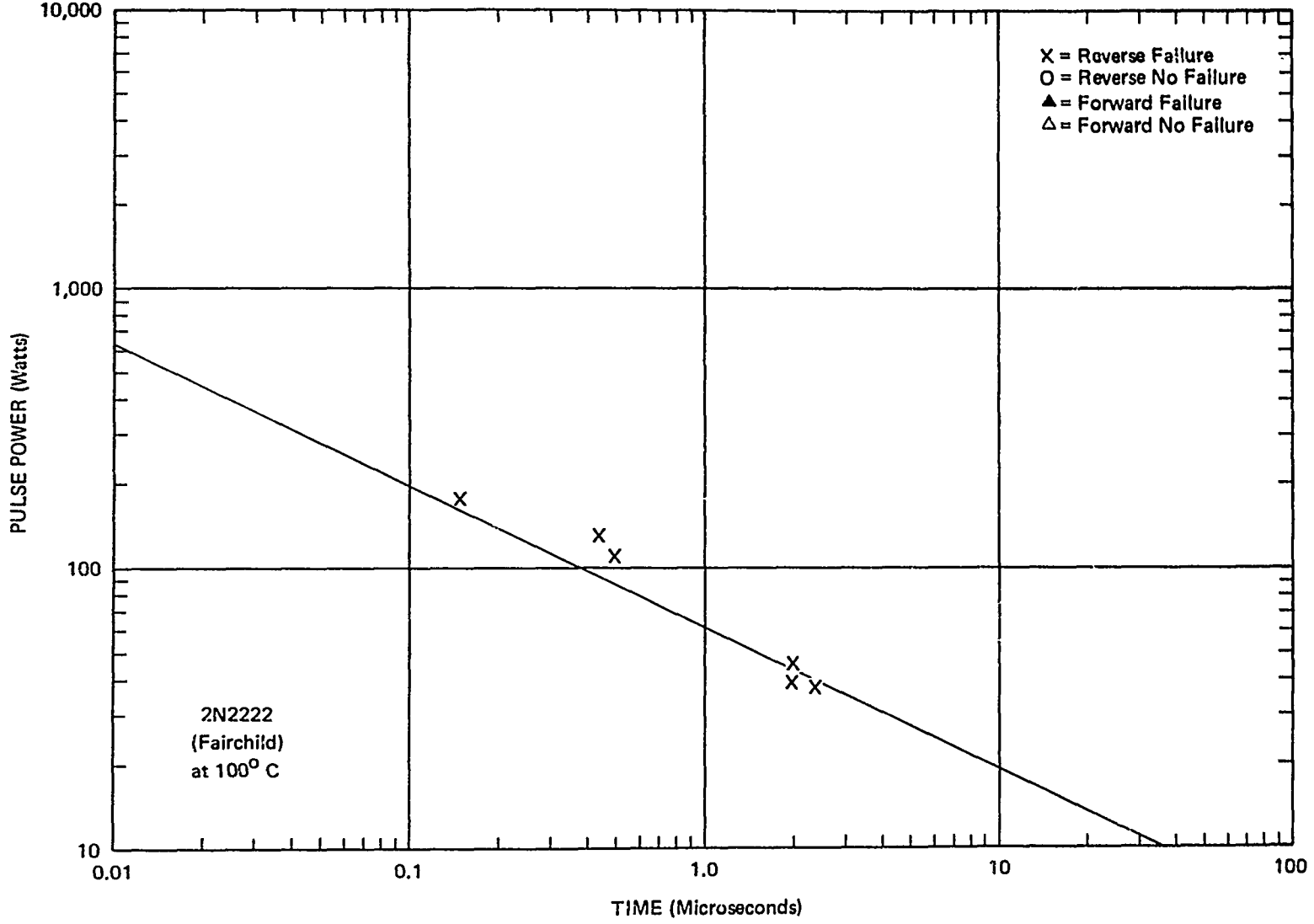
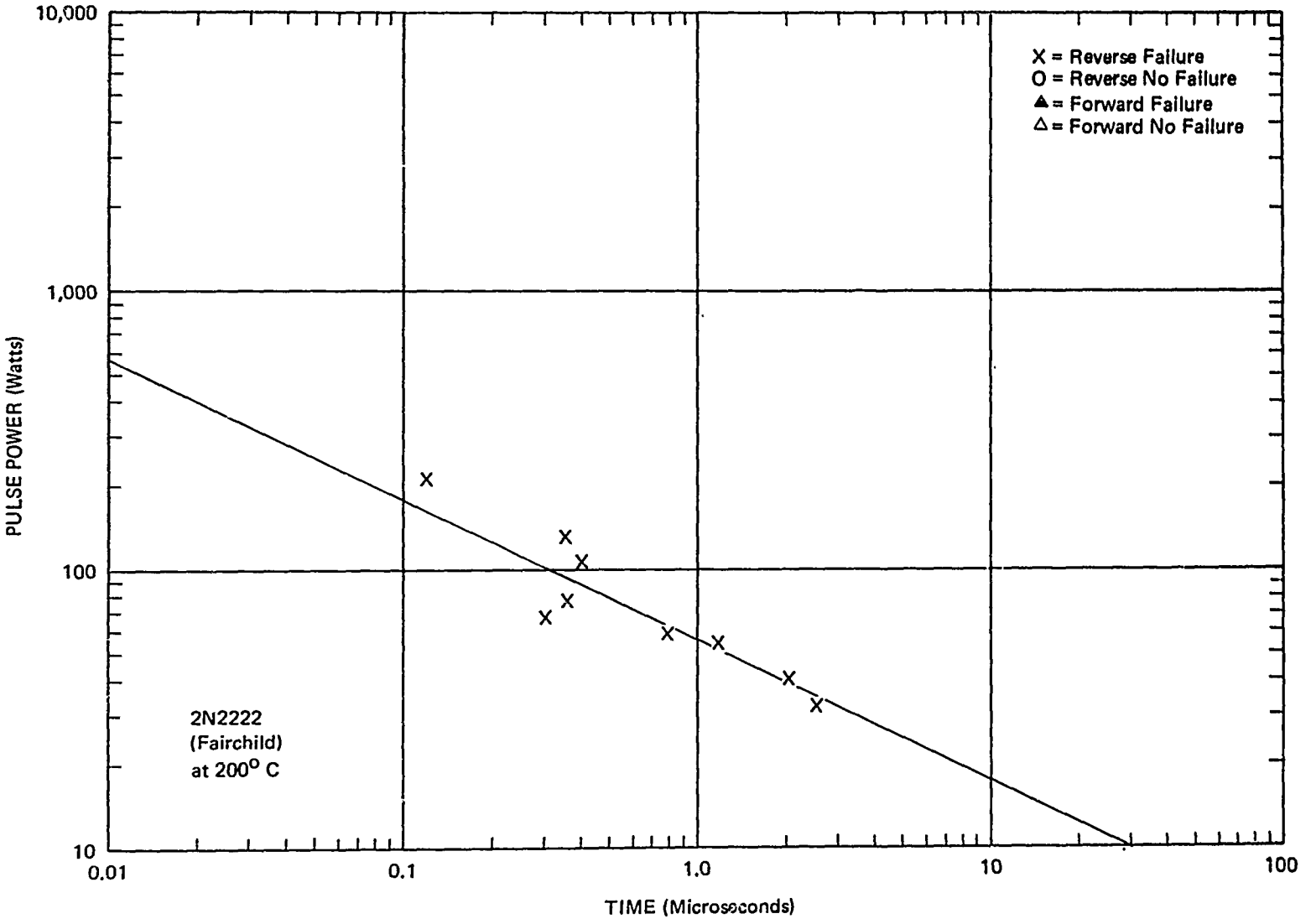
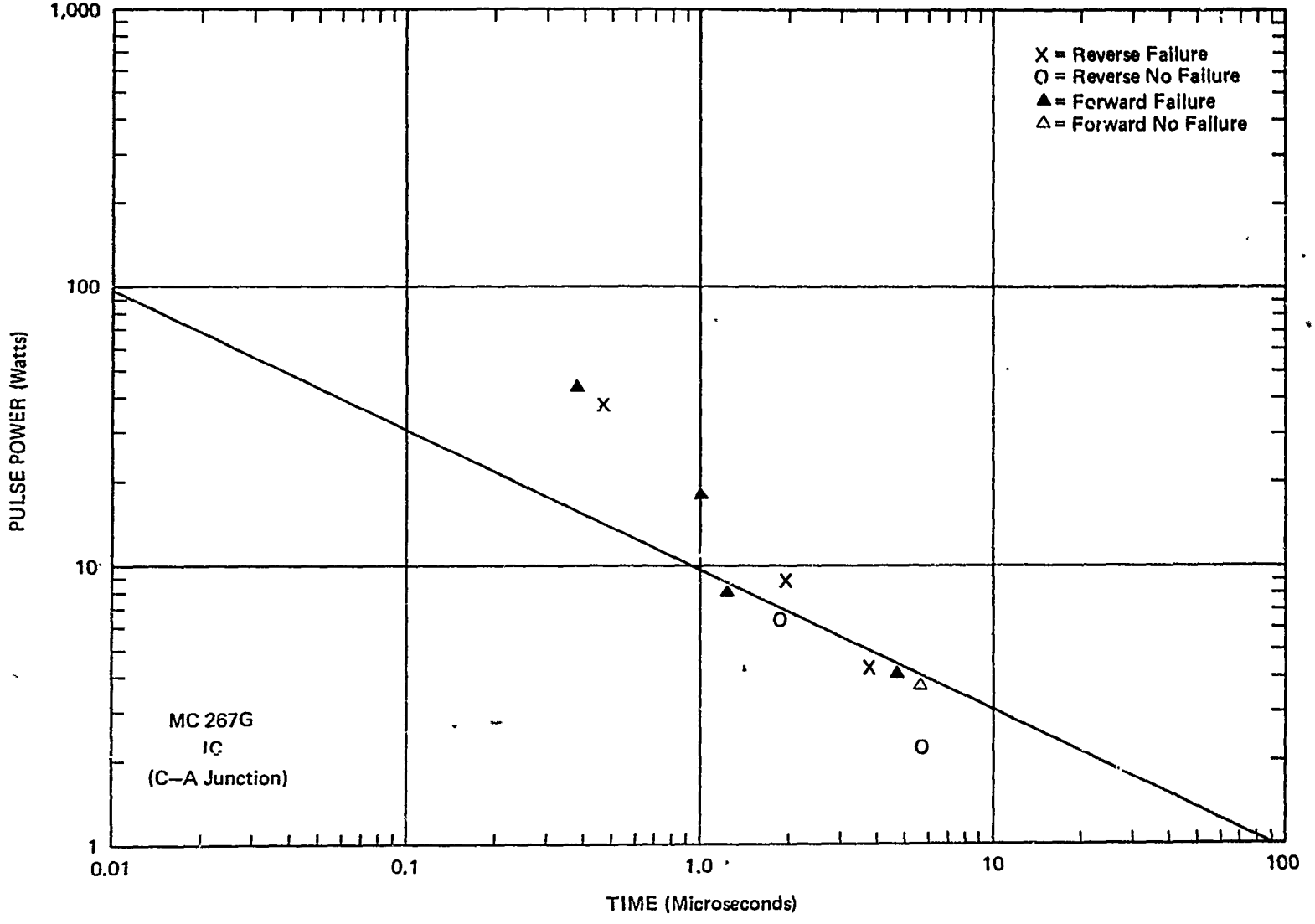
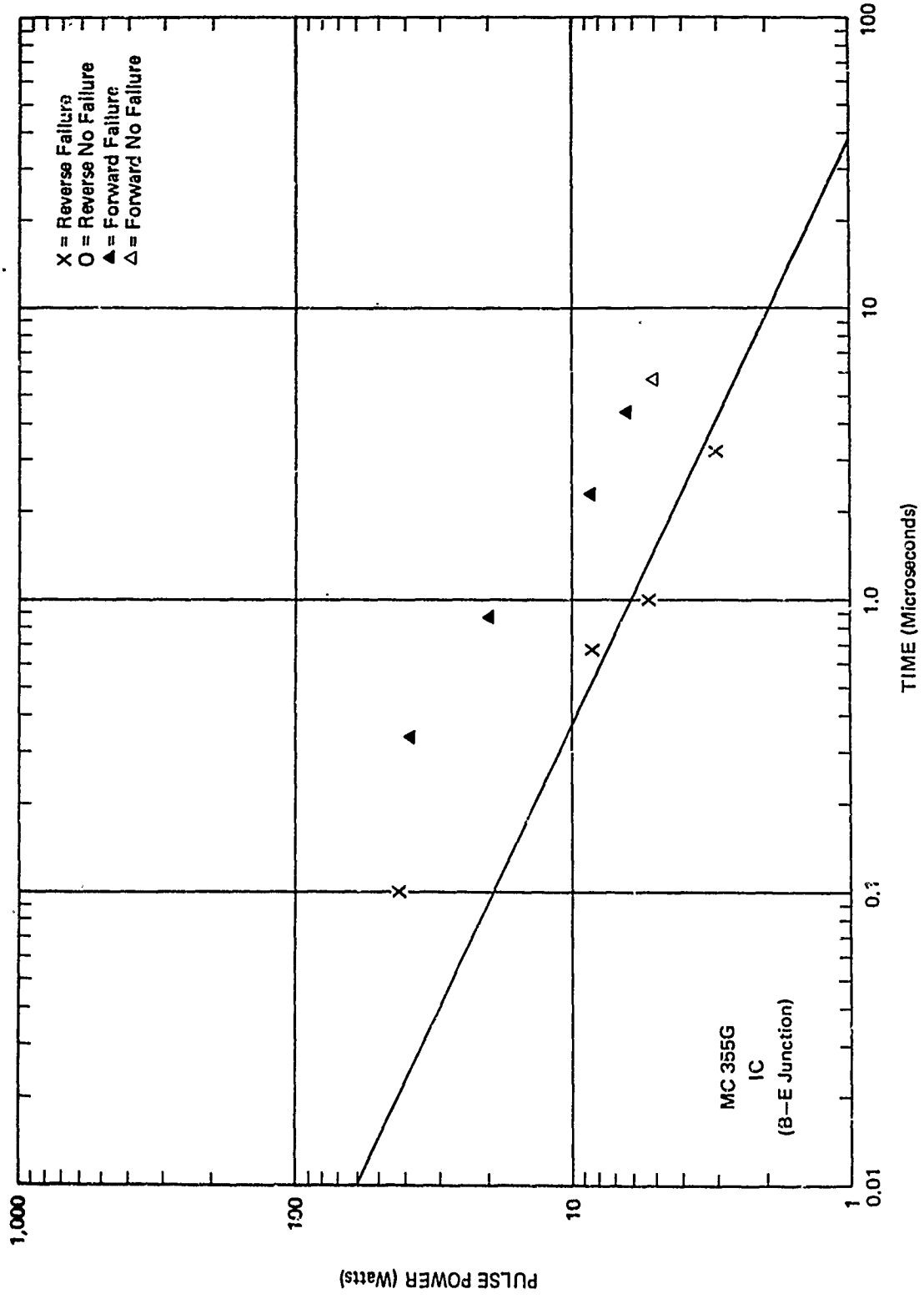
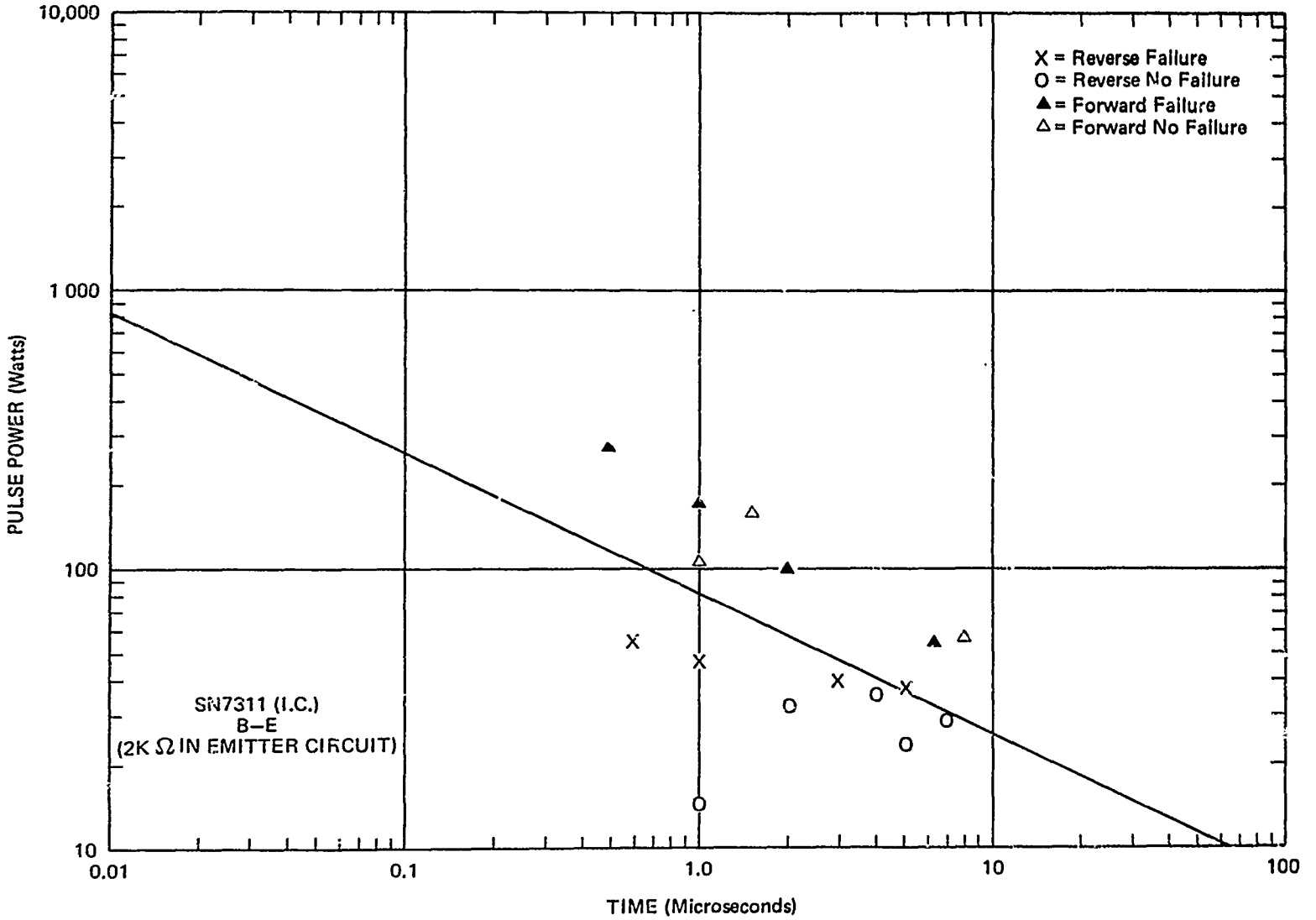
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
T.I.
(C–E)


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
(Fairchild)
at 100° C


10,000
1,000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
2N2222
(Fairchild)
at 200° C


1,000
100
10
1
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MC 267G
IC
(C–A Junction)


X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
MC 355G
IC
(B–E Junction)
PULSE POWER (Watts)
1,000
100
10
1
0.01
0.1
1.0
10
100
TIME (Microseconds)


10,000
1 000
100
10
0.01
0.1
1.0
10
100
PULSE POWER (Watts)
TIME (Microseconds)
X = Reverse Failure
O = Reverse No Failure
▲ = Forward Failure
△ = Forward No Failure
SN7311 (I.C.)
B–E
(2K Ω IN EMITTER CIRCUIT)